Enabling At-Speed Testing of 112 Gbps

ATE for Characterization & HVM
Contents

- Introduction
- MultiLane products
- Application examples
- PAM4
- De-embedding of channel effects
- Calibration
- Business model
- Summary
Company Profile

- Highly Agile and Innovative Company
- First to market with high value solution for HSIO testing
- > 200 released products
- > 500 customers
- > 50% CAGR for 8 years
Worldwide Customers
ML’s High Speed IO Testing Capability

Time Domain Analysis

Frequency Domain Analysis
HSIO Applications

Communication Interfaces – New Speeds Driving Risk & Opportunity

- Internet infrastructure (PAM4 @ 100, 200, 400 Gbps)
- Photonic components (Trans-Impedance & Variable Gain Amps)
- High-Speed Analog devices
- Proprietary SerDes Interfaces

Computer Interfaces - The Need for Speed continues:

- PCIe Gen4 → PCIe Gen5 (32 Gbps x8/x16)
- USB 3 → USB 4 (40 Gbps, 2-Lane)
- Display Port1.4 => 1.4a (32.4 Gbps, 4-Lane)
- HDMI 2 => HDMI 2.1 (48 Gbps, 4-Lane)
MultiLane ATE Strategy

2018
Instruments used to be integrated in load boards

2019
Instruments re-formed to become a V93000 Test-head Extender

2020
Lane count increased from 64 to 512
Overview of the V93K/MultiLane HSIO System

You can apply the Twinning solution to the compact test head (CTH) equipped with the Enhanced DUT Scale Interface only. The Multilane® Modules reside on the family board inside of the base frame. These signals are then routed to the DUT board through the family board and base frame pogo pins.

To the right shows the V93000 CTH with Twinning including the family board and base frame installed.
Twinning Features & Benefits

Integrated docking solution for a “mother/daughter” board approach including power, control and mechanics for customized test solutions

Values

- Increase space for user defined components (on PCB) and modules in a production environment
- Gives flexibility for the distribution of tester resources on DUT interface
- Fully compatible
- High level of integration into tester environment
  - Customer defined modules
  - External instruments

- Distance between lower level PCB (Family board) top-side and upper PCB (DUT board) bottom-side
  ~ 80mm
- Electrical connection between Family board & DUT board with pogo pins
  - 16 pogo segments
  - 513 pogo pins each
  - Total 8208 pins
Modular Configuration Wafer Sort & final test

- Four Cassettes can fit in the Twinning Frames, (two on each side)
- 2x 4-channel Instruments per cassette
- Tester can be configured for up 32 Lane BERTs
Appendix Instruments

- ML Instruments Specs
- ML Instruments Integration in V93K
- ML Mechanical & Thermal Solution
- ML Software
- ML Applications
- ML Instruments Calibration
# MultiLane Products

<table>
<thead>
<tr>
<th>Product</th>
<th>Description</th>
<th>Bandwidth Coverage</th>
<th>Availability</th>
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<tbody>
<tr>
<td>AT4025-50</td>
<td>4-Lane DSO</td>
<td>50 GHz</td>
<td>Now</td>
</tr>
<tr>
<td>AT4039D</td>
<td>4-Lane BERT 28 GBd PAM/NRZ</td>
<td>24-30 GBd</td>
<td>Now</td>
</tr>
<tr>
<td>AT4039E</td>
<td>4-Lane BERT 56 GBd PAM/NRZ</td>
<td>24-30 and 50-58 GBd</td>
<td>Now</td>
</tr>
<tr>
<td>AT4039EML</td>
<td>4-Lane SE BERT 56 GBd PAM/NRZ w/EML Driver</td>
<td>24-30 and 50-58 GBd</td>
<td>Now</td>
</tr>
<tr>
<td>AT4079B</td>
<td>8-Lane 1 – 30 GBd PAM/NRZ</td>
<td>1 – 30 GBd</td>
<td>Now</td>
</tr>
<tr>
<td>AT4039B-JIT</td>
<td>4-Lane BERT 30 GBd NRZ Jitter Injection</td>
<td>1 – 30 Gbps</td>
<td>Q1 ’20</td>
</tr>
</tbody>
</table>
AT4039D Specs

ATE Firmware 10x Faster than Benchtop

**PPG Features**
- Quad 22 – 29 GBd PAM-4
- Quad 9 – 14 & 22 - 29 Gbps NRZ
- High-speed clock out < 7 GHz
- Gray coding, polarity inversion
- PRBS 7, 9, 13, 15, 23, 31, 58
- PRBS 13Q, 15Q, 31Q
- SSPRQ, square & Custom pattern
- Up to 1500 mVppd voltage swing

**ED Features**
- Error insertion
- Pre and Post-emphasis
- Pre and Post-emphasis, DSP based
- Patterns are generated algorithmically
- Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed
- FFE Equalizers
- > 13 dB equalization with FFE+CTLE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS 7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recover
- BER counters
AT4039E Specs
ATE Firmware 10x Faster than Benchtop

PPG Features
- Quad 23 – 29 & 46 – 58 GBd PAM-4 or NRZ
- High-speed clock out to 7 GHz
- Gray coding, polarity inversion
- PRBS 7, 9, 13, 15, 23, 31, 58
- PRBS 13Q & 31Q
- SSPRQ, square & Custom pattern
- Up to 800 mVppd voltage swing
- Error insertion
- Pre and Post-emphasis
- Patterns are generated algorithmically
- Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed

ED Features
- FFE Equalizers with reflection cancellation and DFE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS 7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recover
- BER counters
AT4039EML Specs

ATE Firmware 10x Faster than Benchtop

PPG Features

- Quad 23 – 29 & 46 – 58 GBd PAM-4 or NRZ
- Single-ended high swing output for EML driving
- Integrated bias-Tees
- High-speed clock out to 7 GHz
- Gray coding, polarity inversion
- PRBS 7, 9, 13, 15, 23, 31, 58
- PRBS 13Q & 31Q
- SSPRQ, square & Custom pattern
- Up to 1800 mVppd voltage swing
- Error insertion
- Pre and Post-emphasis

ED Features

- FFE Equalizers with reflection cancellation and DFE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS 7, 9, 13, 15, 23 & 31 checker
Introducing the Twinning Concept

V93000 Load board with Stiffener
PCB size: 581.66mm x 429.26mm

Twinning Load board with Stiffener
PCB size: 598mm x 480mm

Twinning Pogo Block

Load Board

Family Board

DUT

PCB size: 598mm x 480mm
Docking Steps

- Screw Base Frame on Family Board
- Put Assembly on Tester and dock it
- Put Load Board on and dock it via pneumatic
Multilane V93K HSIO Solution

- Runs independent of tester
- Scalable/Modular
- Blind-mate Interface
- Hard Dock
Full customization of the twinning DUT board will enable either wafer probe testing or package testing.
Appendix Mechanical & Thermal
Cooling System Isolated
Cooling System Integrated
Cooling System Integrated
Mechanical Overview
Appendix Software
SmarTest Integration Model

User Test Program

MultiLane API Library

SmarTest 7.x.x

RedHat 5.0 or 7.0

Windows based tools for MultiLane products

12V Power Supply

Ethernet Router
Software Integration

- ML Shared Libraries for RHEL5 and RHEL7
- Support Multisite Testing.
- SMARTEST sample code available
- High throughput features
- Co-development with Advantest
Software Integration

- SMT Test Flow for stand-alone test procedure with pass/Fail criteria.
- SMT Self Test Capability (RD/WR General Status, temperature, PS voltages, PLL lock status, etc.).
Software Integration

- Signal Analyzer
- Shmoo Plot
- Data Logs
Throughput BERT

BERT Throughput

Setup time (done once) = 424 ms + 1000 ms
settling time
Measurement time = \(\sim 80\) ms

```
[all sites]: Enable Real Time BER and Check Lock Status:  OK
[all sites]: __Enable BER = 1058.621 ms
[site 1, pin PCIRX1p]: Read Lock Status:  1
  ... sleeping BER measuring time:  1 sec
[all sites]: Read Real Time BER :  OK
[site 1, pin PCIRX1p]: BitError :  0
[site 1, pin PCIRX1p]: Spent Time : 1006
[site 1, pin PCIRX1p]: BER : 0.00000000000000e+00
[all sites]: __Read BER = 10.181 ms
[all sites]: Disable Real Time BER on all channels :  OK
[all sites]: __Disable BER = 12.691 ms

[site 1]: Bert Configure TX Line Rate =  OK
[site 1]: __Bert Configure TX Line Rate = 309.563 ms
[site 1]: Bert Configure RX Line Rate =  OK
[site 1]: __Bert Configure RX Line Rate = 0.19 ms
[site 1]: set TX Pattern =  OK
[site 1]: set RX Pattern =  OK
[site 1]: set RX Invert =  OK
[site 1]: __Bert set Pattern = 33.752 ms
[site 1]: set OutputLevel :  OK
[site 1]: __Bert set OutputLevel = 13.715ms
[site 1]: tapsLearned:  0
[site 1]: TM_7Taps:  No
[site 1]: TM_LearnedTaps:  No
[site 1]: set MainTapVal:  1
[site 1]: __Bert setMainTap = 15.192ms
[site 1]: set PreEmphasis :  OK
[site 1]: __Bert set PreEmphasis = 25.823 ms
[site 1]: set PostEmphasis :  OK
[site 1]: __Bert set PostEmphasis = 25.579 ms
[site 1]: __Bert Configure OVERALL = 424.271 ms
```
Throughput DSO

DSO Throughput

Configure measurement time (done once) = **2.2 s**

Measurement time = **638 ms @ 32k samples**

DSP is run in the background if required while the next measurement is taking place.

```plaintext

[site 1, pin 'PCIRX2DSO']: DSO Temp [degC] : 35
[site 1, pin 'PCIRX2DSO']: DSO Firmware rev : 1.6
[site 1, pin 'PCIRX2DSO']: DSO Board Id : 4744
[site 1, pin 'PCIRX2DSO']: DSO SN : 198306130531
[site 1]: timer get SN of DSO = 0.043 ms
[site 1]: Configure DSO : OK
[site 1]: Configure DSO = 2274.097 ms

```

[all sites]: DSO averaging factor: 0
[all sites]: Get Data: OK
[all sites]: __Get Data = 638.134 ms
Appendix Applications
### Applications

<table>
<thead>
<tr>
<th>Category</th>
<th>Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Diff-Diff TIA/Driver Test</strong></td>
<td>- 4x56GBd AT4039E/4x28GBd AT4039D&lt;br&gt;- AT4025</td>
</tr>
<tr>
<td><strong>SE-Diff TIA/Driver</strong></td>
<td>- 4x56GBd AT4039EML&lt;br&gt;- AT4025</td>
</tr>
<tr>
<td><strong>Diff-Diff and SE-Diff TIA/Driver with CDR</strong></td>
<td>- AT4039E/AT4039D/AT4039EML</td>
</tr>
<tr>
<td><strong>ASIC with High-speed IO</strong></td>
<td>- AT4039E/AT4039D&lt;br&gt;- AT4025</td>
</tr>
</tbody>
</table>
ATE Application Examples

ASIC Test

Multilane AT-series BERTs / TDRs

ASIC
With
High Speed IO

Multilane AT-series DSOs
ATE Application Examples

TIA Test

Multilane AT-series BERTs / TDRs

Multilane AT-series DSOs

Multilane AT-series BERTs

TIA/Driver

PRBS

PPG

PRBS

TIA/Driver

CDR

PRBS

TIA/Driver

EDR

Multilane AT-series BERTs
SE and Diff TIA measurements

Eye/Pattern Measurements

Eye captures allow to visualize non-linearities and imbalances.

BER versus input power is a typical amplifier test to ensure the DUT will work error-free over the intended range of inputs.

- Eye Diagram
- Pattern
- Jitter Decomposition
- Histogram
- Filters / Equalizers
- De-embedding
- PAM4 Meas.
Sample TIA S-Parameters vs. Gain

Variable Gain Amplifiers and TIAs have outputs that linearly vary with inputs over a given range.
Some RF amplifiers and TIA have a Bandwidth control input and its effect must be characterized.
TIA Linearity Measurements

Measurements on Sample TIA

RLM

THD
Appendix Calibration
Calkit Top View

Calkit has load board form factor
- It contains all the cables and brackets for quick mount
- Simply undock load board and mount calkit instead
- No need to touch the ML cassettes
- Quick connect to external calibration reference ML4035
- ML4035 cabling de-embedded
Ganged Connectors

Rosenberger SMPM-BM to SMPM Right-angle

Custom Brackets

SMPM to K Adapters

Standard K cables

to ML4035

From Cassette
1- Path verification using TDR
2- Path ISI compensation using 7-taps FFE in ML4035 DSO
3- Amplitude calibration of PPG using ML4035 DSO
Calibration – DSO to DUT Path Compensation

1- Path verification using TDR
2- Amplitude calibration of DSO using ML4035 PPG
Example of De-embedding using a Scope

DSO measures and de-embeds the channel in frequency domain.

DUT signal after compensating for the trace losses.
Business Relationship

The needs of the high-speed IO (HSIO) testing community are very specialized. Similarly, the needs of the semiconductor test community are very diverse and specialized.

In 2018, Advantest (a leading supplier of SOC test systems) together with MultiLane (a leading supplier of HSIO test instruments) started to explore partnering together to provide a single platform solution which leverages the best capabilities and qualities of both our companies.

The concept was straightforward. Existing MultiLane instruments were ported to a formfactor compatible with Advantest’s test head extension frame.
Delivery Path for MultiLane Solution

- **Top Side DUT Board**
  - Designed/Sold/Delivered by Alta-Nova & others
  - Note: This “twinning” DUT board is NOT a standard 93K DUT Board

- **Pogo Segment**
  - Sold/Delivered by Advantest

- **HSIO Card Cage**
  - Sold/Delivered by MultiLane

- **Family Board**
  - Designed/Sold/Delivered by Alta-Nova

- **Direct-Dock Direct-Dock Beam (E8016BBWS)**
  - Sold/Delivered by Advantest

- **Instrument Cassettes**
  - Sold/Delivered by MultiLane

- **Wide-Band Interconnect Cables**
  - Designed/Sold/Delivered by e.g. Rosenberger

- **12V power supply, cables, & mounting hardware for attaching to 93K manipulator**
  - Sold/Delivered by MultiLane
Facility Requirements for MultiLane HSIO Solution

- Main Power: 100 .. 240V, 2.8A
- Pressurized Air: ~2 CFM
- Ethernet: 1x GbE link – One MAC address per instrument
- Weight: Twinning frame ~35 Kg
THANK YOU