ML4054-400 Gen2

Technical Reference and user manual

400G production Tester

Innovation for the next generation

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1. General Description

The ML4054-400 is a fully featured 400G BERT with a native CFP8 port. This instrument is used in testing QSFP-DD and OSFP modules through the CFP8 to QSFP-DD or CFP8 to OSFP adapter. These connector savers are suitable for transceiver testing.
The ML4054-400 simplifies production testing by eliminating the external cabling. It is designed for 400G applications.
These passive MSA compliant adapters drive the signals between the CFP8 connectors and QSFP-DD/ OSFP connectors. The ML4054-QDD and ML4054-OSFP support all the QSFP-DD/ OSFP features and pin mappings.

At the receiver side, an octal port CDR device is implemented, able to recover up to 53.125Gbps PAM4 signal or 26.5625Gbps NRZ signal.

The ML4054-400 also supports FEC, three FEC types are currently implemented: RS544, RS528 and Firecode. Supported on both eye modes: PAM4 and NRZ and at high and low rates

2. Ordering information

The ML4054-400 can be ordered with the CFP8-QSFP-DD adapter or with the CFP8-OSFP adapter with the following part numbers.

ML4054-400	ML4054-400 Module Tester
ML4054-QDD	CFP8 to QSFP-DD adapter
ML4054-OSFP	CFP8 to OSFP adapter

Table 1: Hardware ordering information

For more details please refer to the below link:
https://multilaneinc.com/product/ml4054-cfp8/

3. Operating conditions

A 110/220V adapter is used to power-up the board.

Faceplate's LED Indicator:

- PWR LED green: indicates that the board is powered on and able to operate all the measurements.
- T˚ LED red: indicates that the temperature of the board has surpassed the 70˚C value.

In order to prevent overheating, this temperature is considered as the cutoff value.
The instrument will resume normal functionality again once the temperature is within the optimal range.

4. Block Diagram

The ML4054-400 block diagram is illustrated in figure 1 with the CFP8 to QSFP-DD adapter and in figure 2 with the CFP8 to OSFP adapter. Signals are transmitted from the TX side to the adapter through eight independent channels, and the received signals are routed from the adapter side to the RX side of the ML 4054-400. These signals can be monitored and controlled channel by channel. The adapters QSFP-DD and OSFP are MSA compliant.

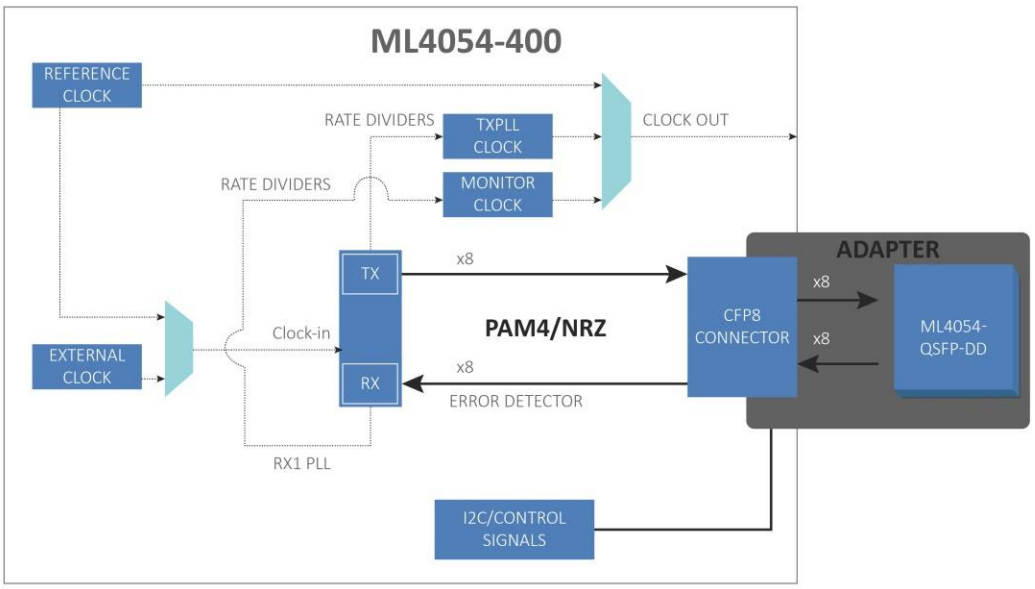


Figure 1: The block diagram of the ML4054-400 with QSFP-DD adapter

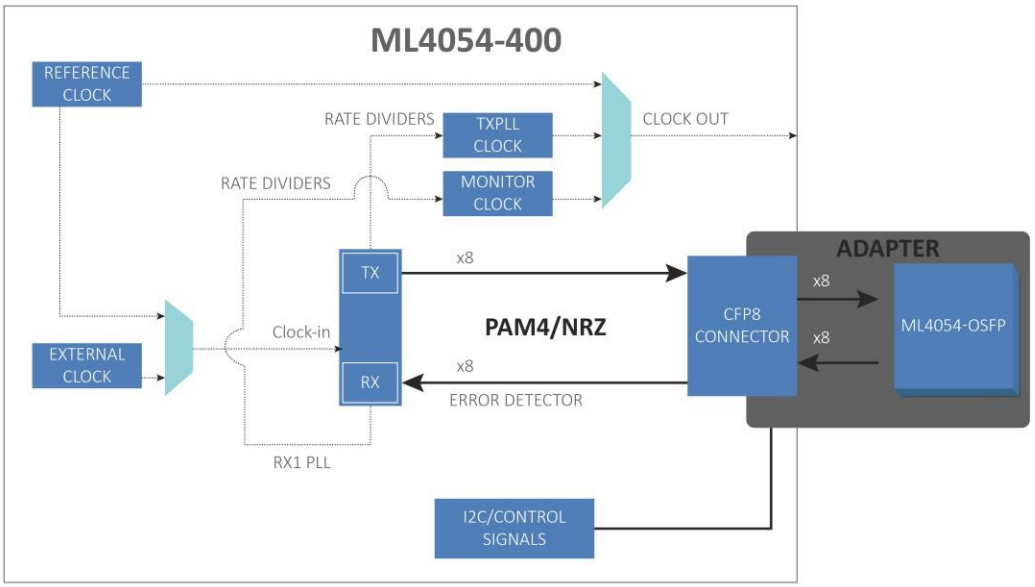


Figure 2: The block diagram of the ML4054-400 with OSFP adapter

5. Channel Signal Integrity

The loss of the PCB traces of ML4054 board, the CFP8 connector and the PCB traces of the adapters for both sides: TX and RX, is shown in figures 3 and 4:

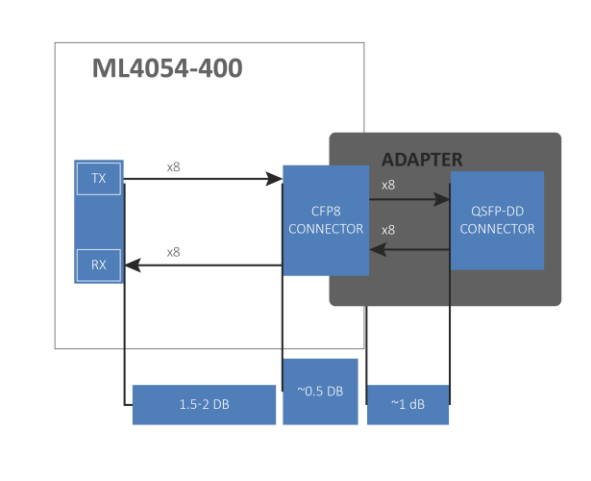


Figure 3: ML4054-400 with QDD adapter trace loss

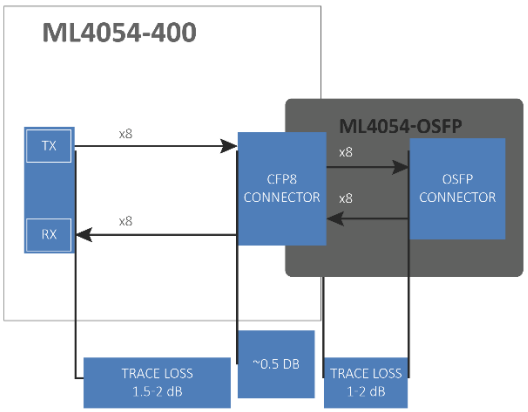


Figure 4: ML4054-400 with OSFP adapter trace loss

With the ML4054-QDD adapter plugged the total loss of the instrument is equal to ~3.5dB.

With the ML4054-OSFP adapter plugged total loss of the instrument is between ~3dB and 4.5dB.

The amplitude calibration is performed at the QSFP-DD or OSFP connector point. The channel losses are compensated after calibration. The calibration procedure takes into consideration, the loss of the additional channel used for calibration, so the amplitude at the connector point would be exactly the same one selected on the GUI.

6. Hardware design overview

Figure 5 shows a general view of the ML4054-400 with QSFP-DD adapter or OSFP adapter.

Figure 5: ML4054-400 with adapter

The instrument dimensions are shown in figures 6 and 7.

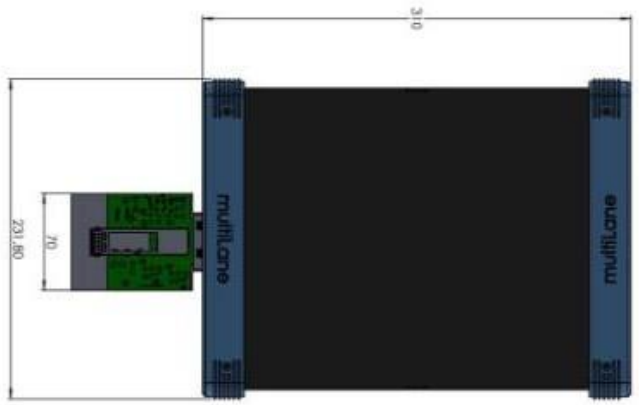


Figure 6 : ML4054-400 top view with dimensions

Figure 7: ML4054-400 front view with dimensions

With an overall weight of two kilograms.
The back plate includes an ON-OFF switch button, Ethernet and USB ports. A 110/220V power adapter can be connected to supply the board with the required power.
The faceplate shows two SMA connectors for clock connection: clock-in and clock-out. And a push button to turn on/ off the instrument.
Once powered up, the switch and push buttons turned on, the board should be able to perform all the required measurements.
The ML4054-400 including the adapter have a total power consumption of 15.6W.

7. Clock Configuration

The ML4054-400 supports input and output clocks. For the Clock out: The user can switch between three options: reference clock, TXPLL clock, and monitor clock.

The monitor clock supports up to around 900MHz differential clock rate. In order to get an optimal eye using the monitor clock, Ch1 should be set in loopback mode and lock, as it will be considered as the CDR that the ML4054 will use to generate the Monitor clock. The available monitor clock rate dividers are 32, 64, 128, 256, 512, 1024, 2048, 4096.

The reference clock supports up to 425MHz with an optimal value of 156.25MHz.
The TXPLL clock, generated by the TX side, varies between Rate/4 and Rate/32. The available rate dividers are 4, 8, 16, and 32.
The analog clock input range varies between 80-700 MHz with an optimal value of 156.25MHz

8. Transmitter side characteristics

As described above the TX signals are transmitted through eight independent channels.
The total loss of the TX channel with the adapter is up to ~3.5 dB if the QSFP-DD adapter is connected, and up to 4.5 dB if the OSFP adapter is connected.
Although the amplitude calibration is performed at the adapter's connector, the channel used for calibration, is being de-embedded to compensate the additional loss, in a way that the output amplitude will be same as the one selected on the GUI.
The optimal settings for each channel, generated during the calibration process, are being applied on high and low rates, and in both eye modes: NRZ and PAM4.
These settings, once applied and saved, ensure that ML4054-400 performs all the required measurements.
These settings can be controlled by the user in advanced mode.
In this way the user can control all the TX settings including: TX pattern, amplitude, the 3 FFE taps Pre-emphasis, Main-Tap, Post-Emphasis or the 7 FIR taps… The Outer and Inner level of the PAM4 eye can be adjusted in advanced mode.

The ML4054-400 operates in PAM4 and NRZ modes, on numerous bitrates.
The BERT locks on all the supported rates, amplitudes and patterns. The parameters are mentioned in table 2.
The TX Equalization is a digital combination of FFE and DFE, PAM4 gray coding. Test pattern generator per lane includes error injection.
The patterns, error insertion and emphasis taps can be checked and controlled per lane.

Kindly refer to the user manual page 14 for more details to operate the ML4054-400.

Table 2 shows the TX Output Characteristics of the ML4054-400.

Parameter			Typical	Maximum	Unit
Line Rate	NRZ		1.12 -1.56 2.24- 29.4	up to 29.4	Gbps
	PAM4		1.12 -1.56 2.24- 29.4	up to 29.4	Gbaud
Clock-out Amplitude			TBD		mV
Clock-out Frequency	Monitor		Rate/4096 – Rate/32	up to around 900	MHz
	TXPLL		Rate/32 – Rate/4		
	Reference		156.25		
Output Amplitude	Low Rate (NRZ & PAM4)	Advanced Mode	Up to 750		mV
		Optimal Settings Mode	285-610		
	High Rate (NRZ & PAM4)	Advanced Mode	Up to 600		
		Optimal Settings Mode	195-405		
Patterns			PRBS 7/9/11/13/15/23/31 /58/9_4 JP03B, IEEE 802.3bs, OIF-CEI-3.1 User defined		
Loss	with QSFP-DD adapter		3	3.5	dB
	with OSFP adapter		3	4.5	dB
Emphasis Resolution			± 1000		Steps

Table 2: TX output specifications

9. Receiver side characteristics

The receiver side characteristics are described in this section.
The BERT locks on different patterns, with the polarity inversion option. The equalizer can be tuned on a range of around 30 dB, the CTLE slider can be controlled channel by channel. Real-Time BER can be measured. Histograms and SNR shared across all eight channels.

- Octal port CDR, being able to recover up to 53.125 Gbps PAM4 and 26.5625 Gbps NRZ.

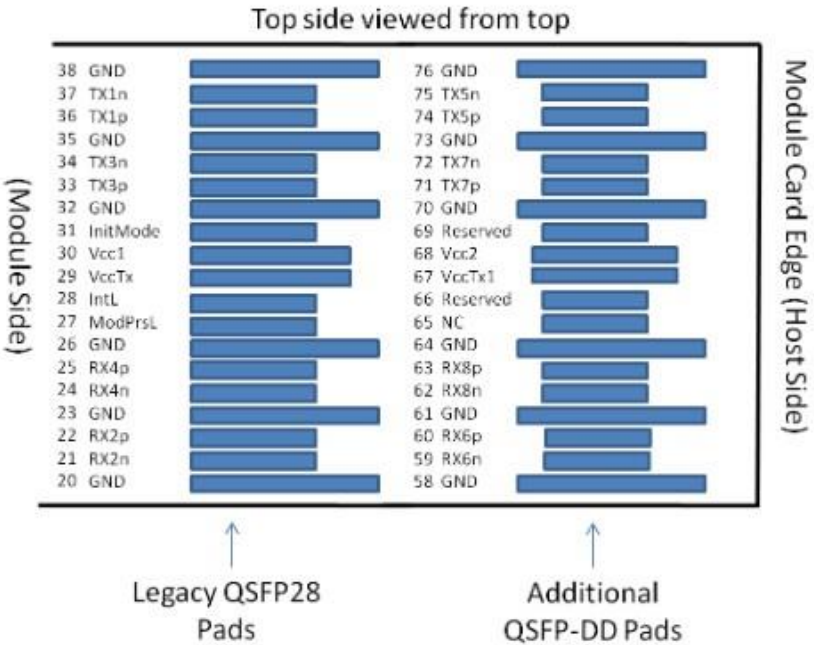
Parameter		Typical	Maximum	Unit
Line Rate	NRZ	1.12 -1.56 2.24- 29.4	up to 29.4	Gbps
	PAM4	1.12 -1.56 2.24- 29.4	up to 29.4	Gbaud
Clock-in Amplitude		TBD		mV
Clock-in Frequency		156.25	80-700	MHz
Sensitivity	Low Rate	80		mV
	High Rate	100		
Patterns		PRBS 7/9/11/13/15/23/31		
Loss	with QSFP-DD adapter	3	3.5	dB
	with OSFP adapter	3	4.5	dB
CTLE			64	Steps

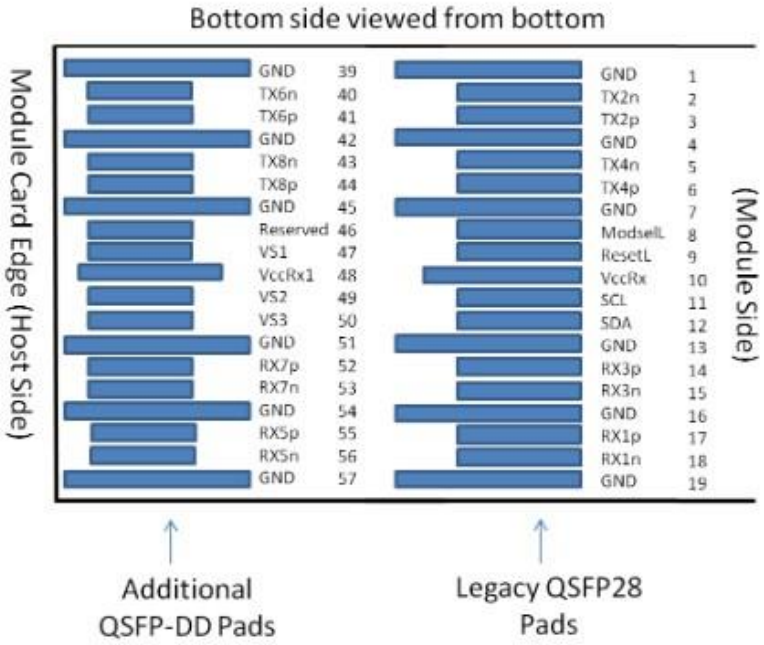
Table 3: Receiver specifications

10. Adapter

10.1 ML4054-QDD Pin Mapping

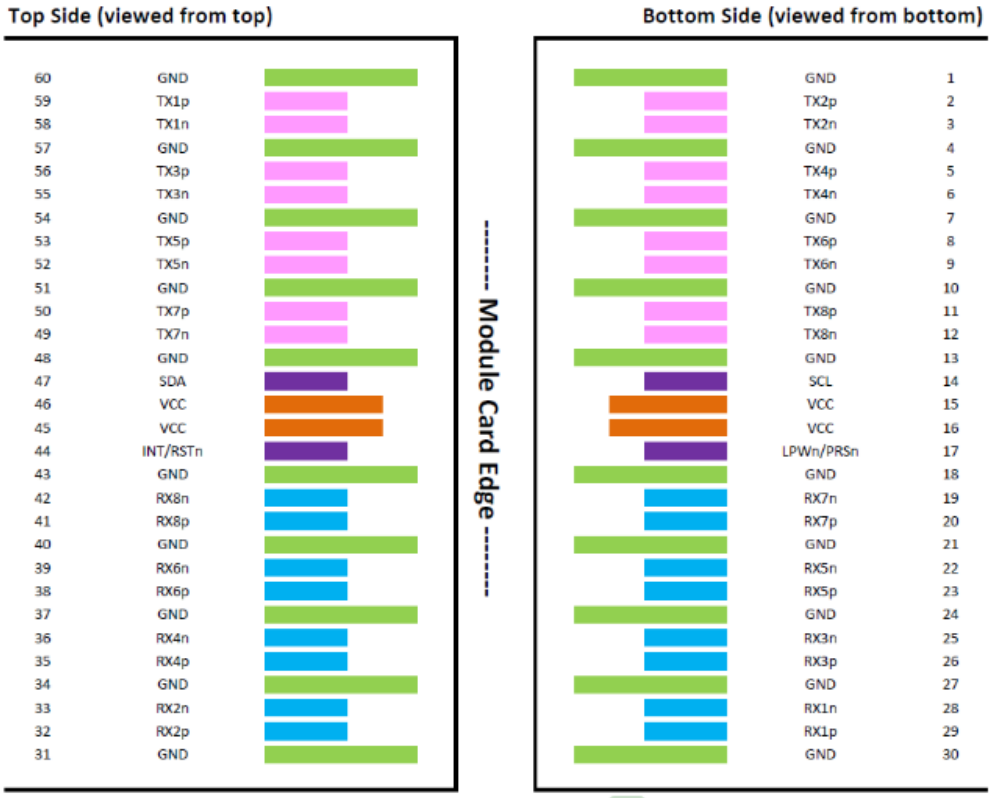
The QSFP-DD adapter pin mapping is compatible with the description mentioned in paragraph 4.1 of the QSFP-DD hardware specifications rev 4.0. Below is shown the pin mapping of the ML4054-QDD adapter.





10.2 ML4054-OSFP Pin Mapping

The OSFP adapter pin mapping is compatible with the description mentioned in paragraph 8.1 of the OSFP Module Specification rev 1.12. Below is shown the pin mapping of the ML4054-OSFP adapter.



11. Low speed signals.

11.1 ML4054-QDD Control and alarm signals

The ML4054-QDD Implements the QSFP-DD low speed pins for control and status. It has the following low speed pins for control and status:

- ModSelL
- ResetL
- InitMode
- ModPrsL
- IntL

They are implemented and driven from a micro-controller with LVCMOS33 logic.

11.2 ML4054-OSFP Control and alarm signals

The ML4054-OSFP Implements the OSFP low speed pins for control and status. It has the following low speed pins for control and status:

- INT/RSTn
- LPWn/PRSn

11.3 I2C signals

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal.
The timing parameters for the 2-Wire interface to the adapter are shown in table

Parameter	Symbol	Typical	Unit
Clock Frequency	fSCL	100	kHz
Clock Pulse Width Low	tLOW	4.47	Us
Clock Pulse Width High	tHigh	5.278	Us
Input Rise Time (400kHz)	tR.400	20	Ns
Input Fall Time (400kHz)	tF.400	22	Ns
Maximum clock stretching		1800	µs

Table 4: Management Interface Timing Parameters

11.4 Supported Power class

The maximum power that the current revision of the adapters, can handle is up to 13.2 W, the hardware is able to ensure stable operation of the QSFP-DD modules up to power class 6, and for the OSFP modules up to power class 4.

12. Current revisions

The revisions of the ML4054-400 and the adapters are listed below:

- 4054-400-RevD_V2_3
- ML4054-QDD RevB1
- ML4054-OSFP_REVB1

All the listed features are tested using the following software and firmware:

- Software revision: 1.8
- Firmware revision: 2.3

13. Future Features

The following features will be implemented in the future ML4054-400 versions:

- Calibrated CTLE slider

14. User Manual

14.1 GUI General Description

This section describes how to operate the ML4054 and all the capabilities of this module tester. The product software is available on the company's website on the below link:

https://multilaneinc.com/ml4054-400/

After installing the setup, the user will be able to open the ML4054-400 GUI.

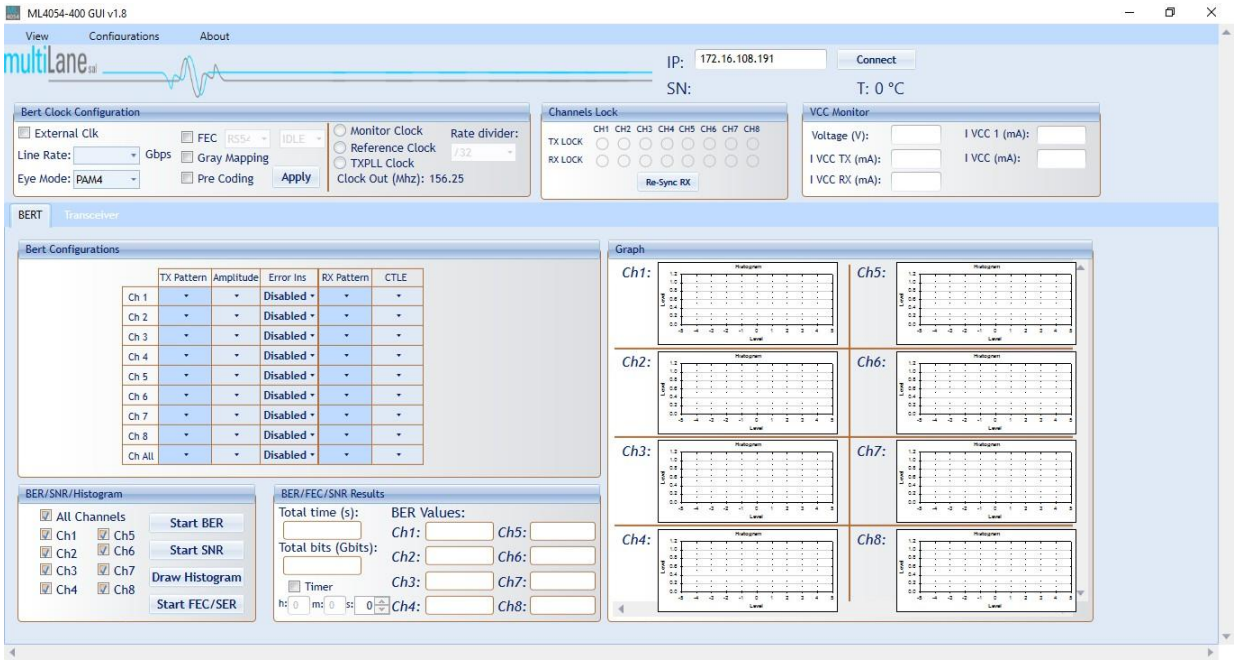


Figure 8: ML4054-400 GUI

14.2 Connecting Procedure

The user needs to connect using the board's IP, after that the board has been powered-up.

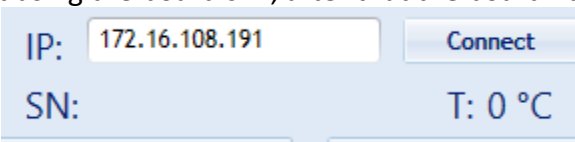


Figure 9: Connecting using the board IP

After clicking on Connect, a pop-up message will appear showing that all the optimal settings that have been saved during calibration are being applied. Also the last used configuration are been applied.

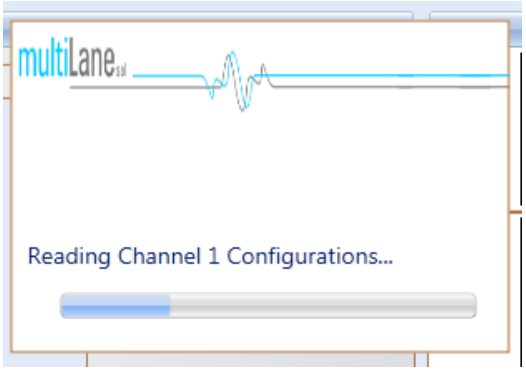


Figure 10: Settings being applied on all channels

Then the user can check all the board's settings including the hardware, firmware and software revisions, by clicking on about.

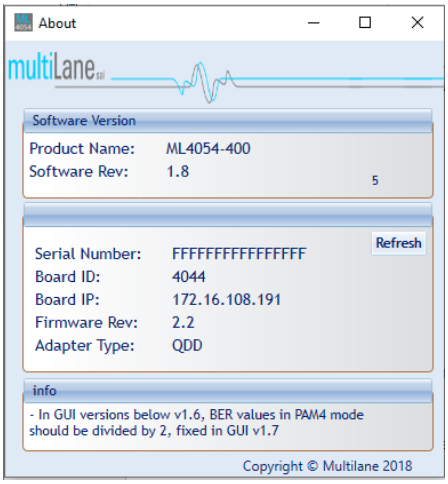


Figure 11: About tab shows the ML4054-400 settings and the adapter's type

The refresh button, helps the user, updating the displayed information whenever any of the fields is being updated.

14.3 BERT Tabs

At the first glance, after connecting to the board, the user will be able to detect on the GUI the: IP, Serial number, monitoring temperature, channels TX and RX lock, and adapter's VCC monitor. Also the user will notice that he can switch between two main tabs: BERT and transceiver.

Figure 12: Main features detected after connecting

The user can select and control all the BERT settings.

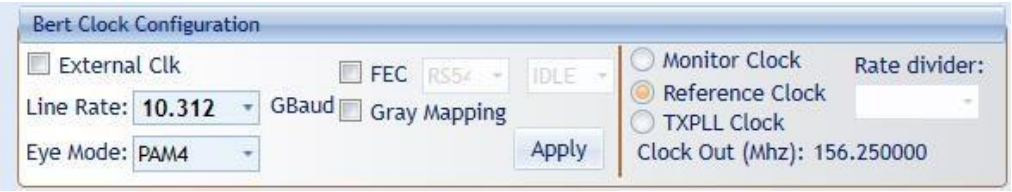


Figure 13: BERT Rate and clock configurations

The ML4054-400 supports both eye modes: NRZ and PAM4.

Figure 14: Supported eye modes

For the clock source, the user can switch between clock-in and clock-out. Whenever the user selects External Clk, after the selection the apply button should be pressed.

If external Clk is selected, which means that an external clock is being provided to the BERT, then the user is notified that the clock input frequency should be appropriate with the selected rate.

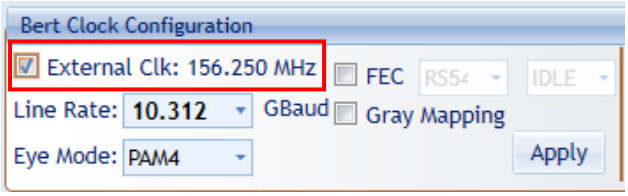


Figure 15: Notification to provide the appropriate clock input and click apply

For the clock-out the user can select reference clock, TXPLL clock out or monitor clock. For the monitor clock the output can be controlled based on the selected clock divider. In order to get an optimal eye using the monitor clock, Ch1 should be set in loopback mode and locked, as it will be considered as the CDR that the ML4054 will use to generate the Monitor clock.

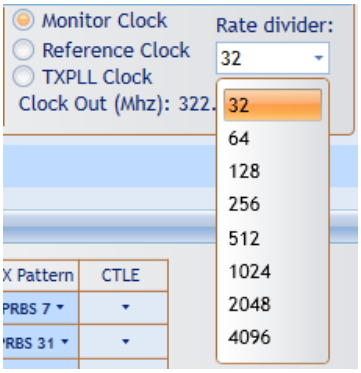


Figure 16: Monitor clock rate dividers

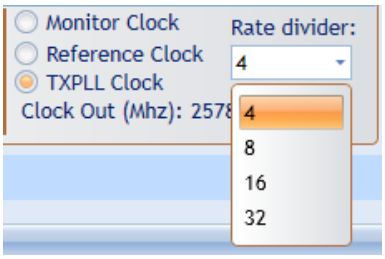


Figure 17: TXPLL rate dividers

For the line rate, the user can select any of the listed rates or enter the desired rate, but this rate should be in the supported range as described in table 2.
The user can control all the BERT configurations, channel by channel.
The user can choose to run this test in the optimal settings mode or in advanced mode.
In optimal settings mode, the optimal settings saved during the calibration process are applied.

	TX Pattern	Amplitude	Error Ins	RX Pattern	CTLE
Ch 1	PRBS 7	497	Disabled	PRBS 7	
Ch 2	PRBS 31	442	Disabled	PRBS 31	
Ch 3	PRBS 31	442	Disabled	PRBS 31	
Ch 4	PRBS 31	442	Disabled	PRBS 31	
Ch 5	PRBS 31	611	Disabled	PRBS 31	
Ch 6	PRBS 31	391	Disabled	PRBS 31	
Ch 7	PRBS 31	442	Disabled	PRBS 31	
Ch 8	PRBS 31	551	Disabled	PRBS 31	
Ch All			Disabled		

Figure 18: BERT side in optimal settings mode

In NRZ mode, for each level the corresponding eye amplitude is detected on the scope.

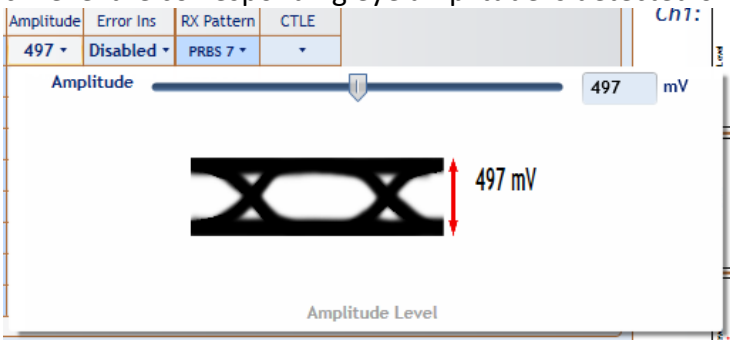


Figure 19: Amplitude control in NRZ mode and with the optimal settings applied

In PAM4 mode, for each level the corresponding total eye amplitude is detected on the scope, this value is equal to the sum of the inner eye amplitude and two outer eye amplitudes. As shown in figure 19.

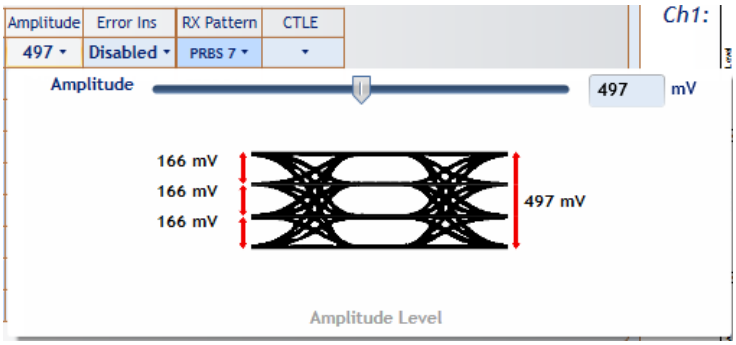


Figure 20: Amplitude control in PAM4 mode and with the optimal settings applied

If the customer desires to control all the parameters, then he needs to go the advanced mode.

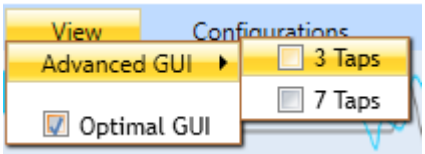


Figure 21: Selecting Advanced GUI

Once Advanced GUI is selected, then the BERT configuration window will be displayed as follows if the 3 taps option is selected:

	TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	Error Ins	RX Pattern	CTLE
Ch 1	PRBS 9	110	-95	747	-157	Disabled	PRBS 9	
Ch 2	PRBS 9	110	-93	731	-176	Disabled	PRBS 9	
Ch 3	PRBS 9	110	-96	741	-162	Disabled	PRBS 9	
Ch 4	PRBS 9	110	-90	731	-179	Disabled	PRBS 9	
Ch 5	PRBS 9	110	-94	736	-171	Disabled	PRBS 9	
Ch 6	PRBS 9	110	-95	739	-166	Disabled	PRBS 9	
Ch 7	PRBS 9	110	-95	726	-179	Disabled	PRBS 9	
Ch 8	PRBS 9	110	-91	761	-149	Disabled	PRBS 9	
Ch All						Disabled		

Figure 22: BERT Configurations in Advanced Mode with 3 taps option

Main-Tap, Pre and Post Emphasis level varies between ±1000. The amplitude slider does not show anymore the values that have been saved during the calibration. The user can go up to 120% and the corresponding amplitude is detected on a scope.
If the 7-taps option is selected, then the user will be able to control the FIR 7 taps instead of the 3 taps. The user can manually adapt the 7 taps to improve the output depending on his application.

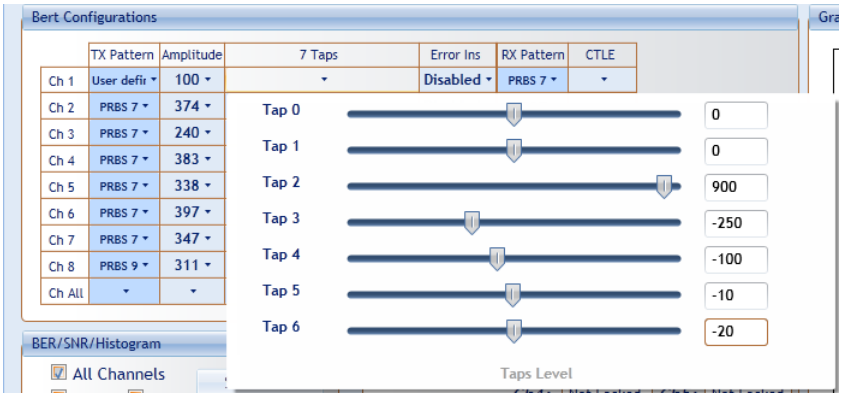


Figure 23: BERT Configurations in Advanced Mode with 7 taps option

The user can test the BER, histogram and SNR, on the selected channels.

Figure 24: BERT tests

While running the BER test, the BER value is shown in the white boxes and on the BER graph is being displayed.

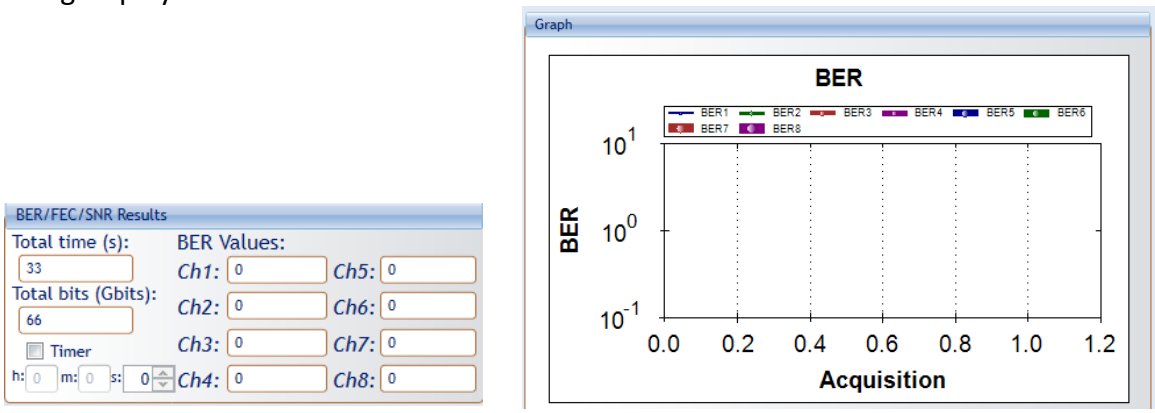


Figure 25: BER display

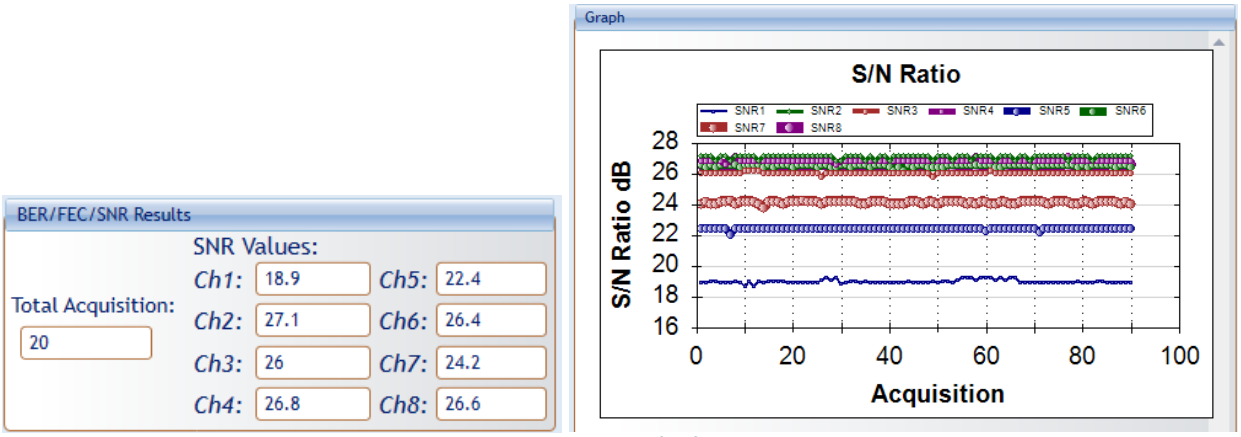


Figure 26: SNR display

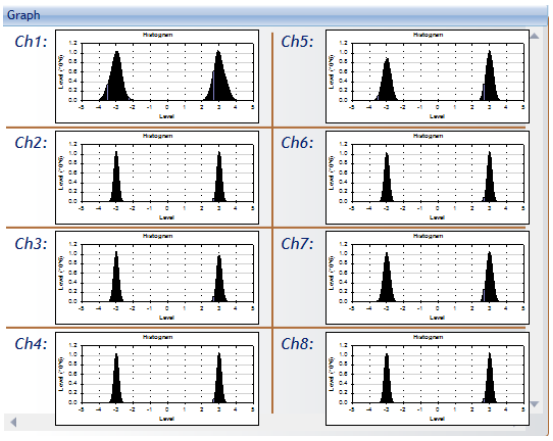


Figure 27: NRZ Histograms

All these measurements can be performed on all the rates, patterns and in NRZ and PAM4 mode. Below are shown some screenshots showing the eye in PAM4 and NRZ modes while channel 1 is being connected to the MLDSO. These screenshots are captured on the highest and lowest amplitude value on low and high rates, with the optimal settings being applied.

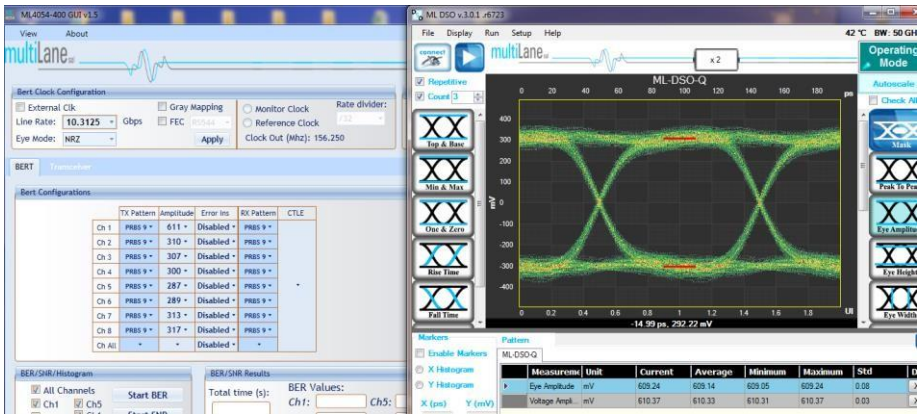


Figure 28: NRZ mode, low rate, highest amplitude on channel 1

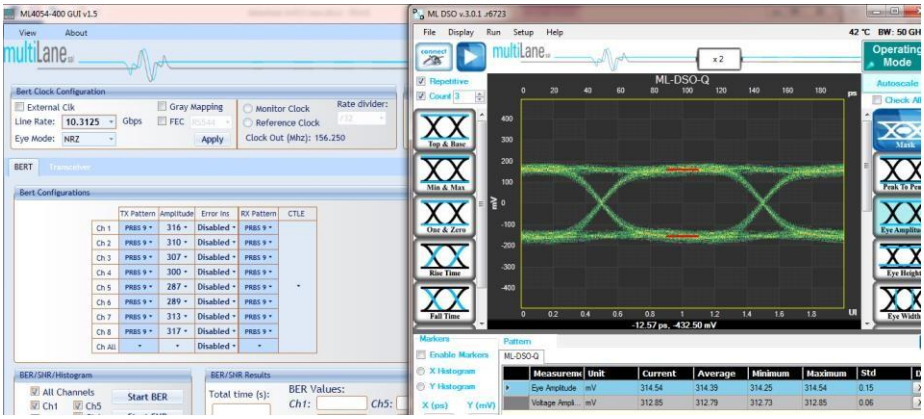


Figure 29: NRZ mode, low rate, and lowest amplitude on channel 1

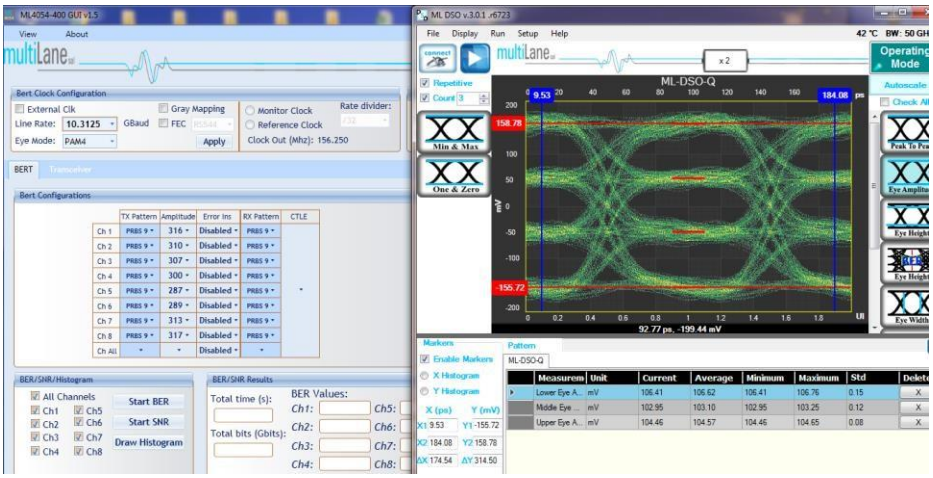


Figure 30: PAM4 mode, low rate, and lowest amplitude on channel 1

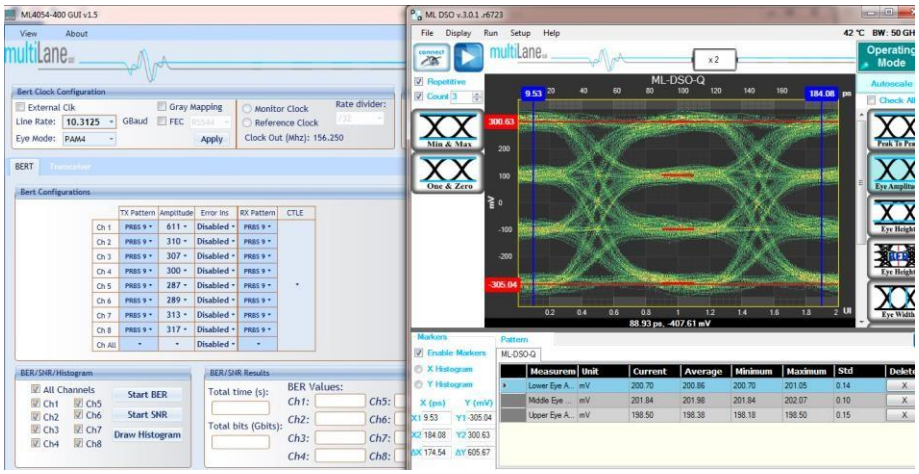


Figure 31: PAM4 mode, low rate, highest amplitude on channel 1

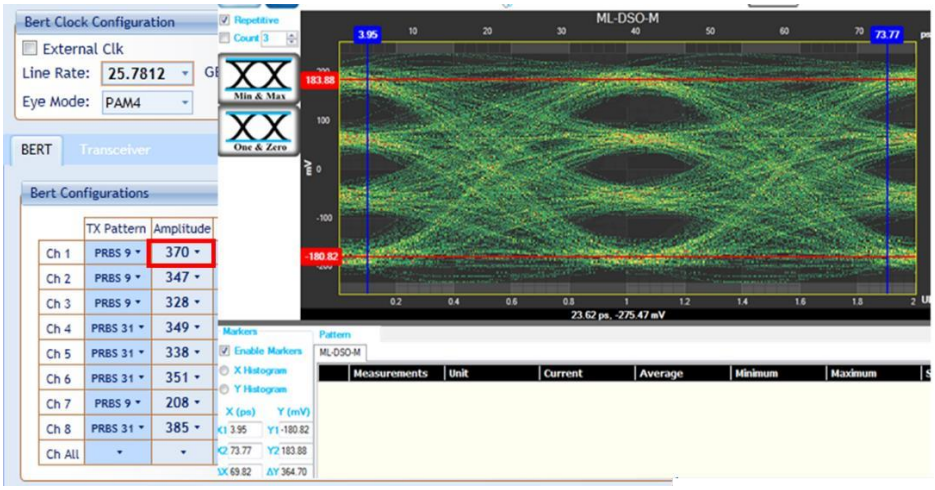


Figure 32: PAM4 mode, high rate, on channel 1

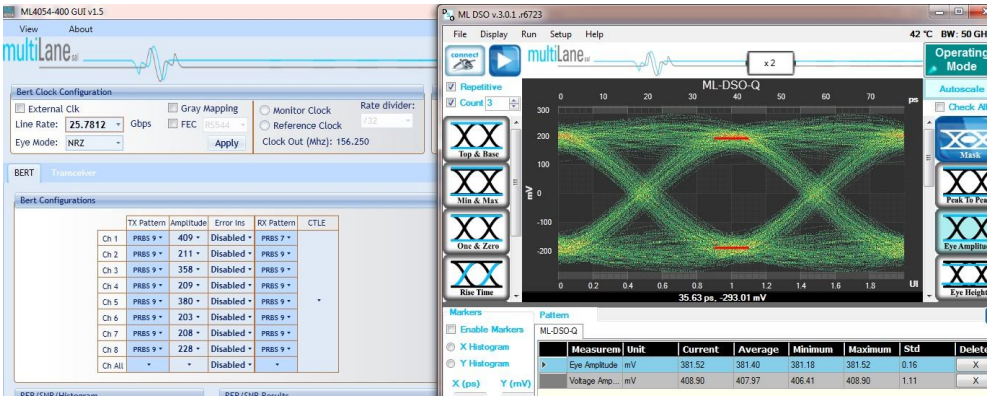


Figure 33: NRZ mode, high rate, and highest amplitude on channel 5

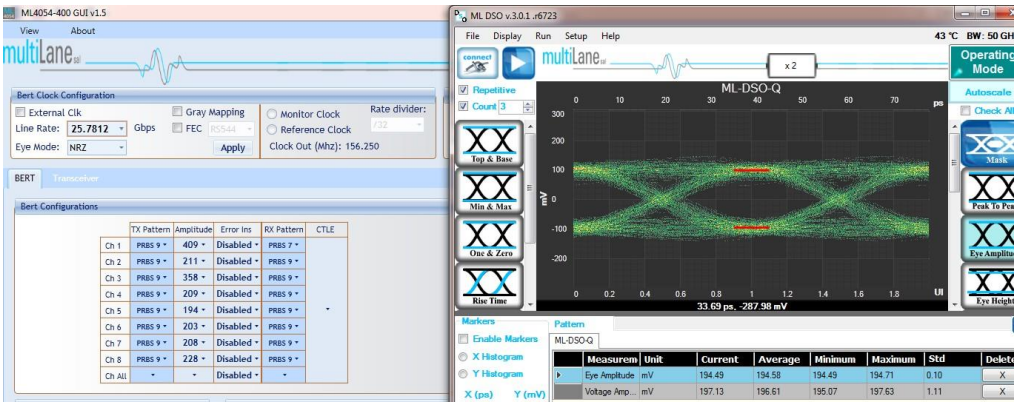


Figure 34: NRZ mode, high rate, lowest amplitude on channel 5

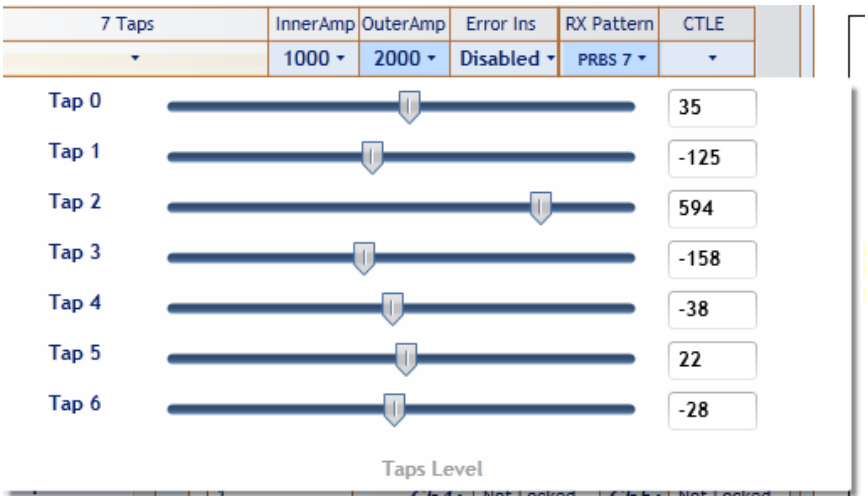


Figure 35: 7 taps used for the below screenshots

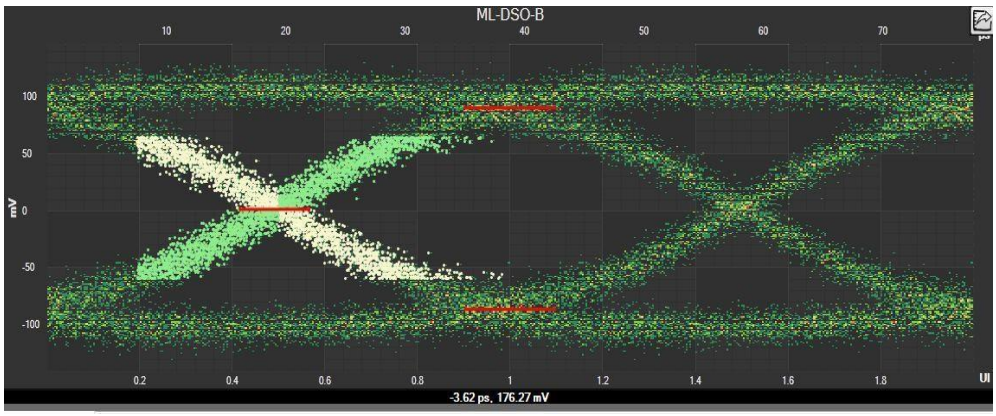


Figure 36: NRZ mode, high rate, with 7-taps FIR on channel 1

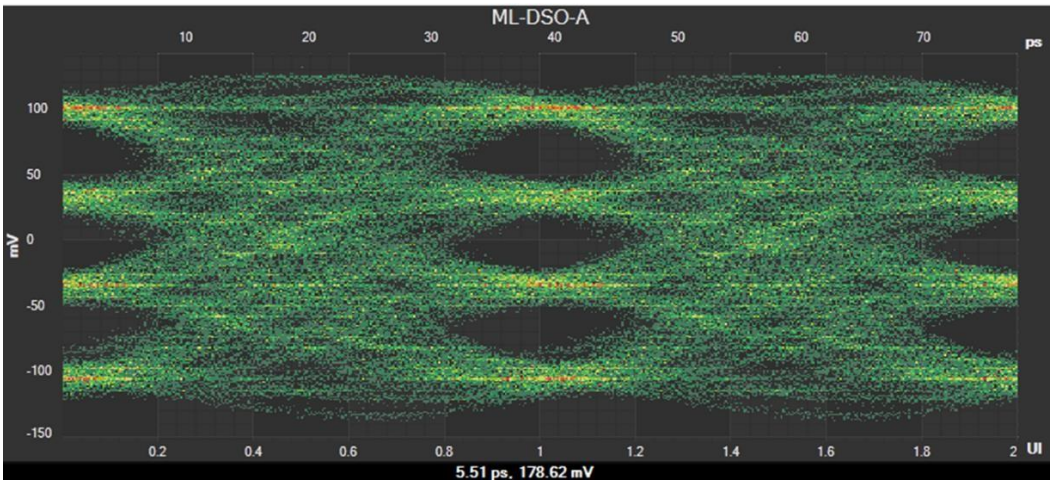


Figure 37: PAM4 mode, high rate, with 7-taps FIR on channel 1

14.4 FEC and SER measurements

The ML4054-400 has FEC support, the three FEC types that are currently implemented are: RS544, RS528 and Firecode. Supported on both eye modes: PAM4 and NRZ and at high and low rates, SER measurement is supported on RS544 and RS528.

To enable FEC the user should checkmark the checkbox next to FEC and then press apply.

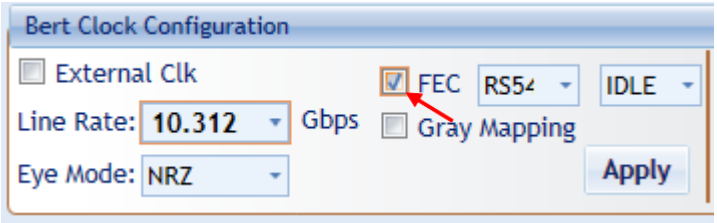


Figure 38: FEC checkbox

The user then chooses the FEC type and FEC pattern, after choosing the type and pattern user should press apply. After applying the user will lose all Rx lock and BERT configurations will be disabled.

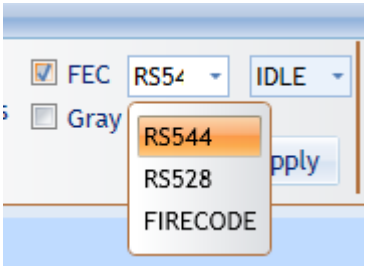


Figure 39: FEC types

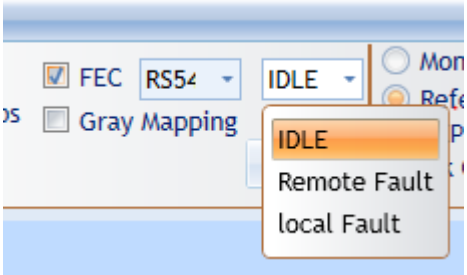


Figure 40: FEC patterns

To start FEC/SER measurement the user should select the desired channels and then press start FEC/SER:

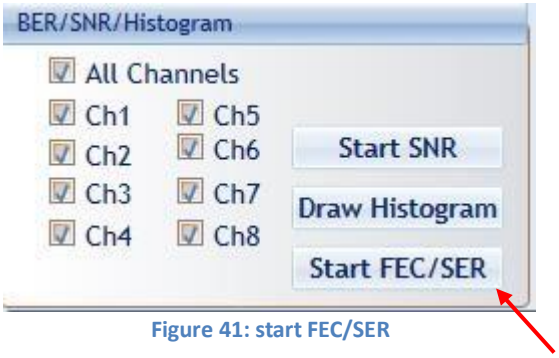


Figure 41: start FEC/SER

RX lock status is updated once FEC measurement has started:

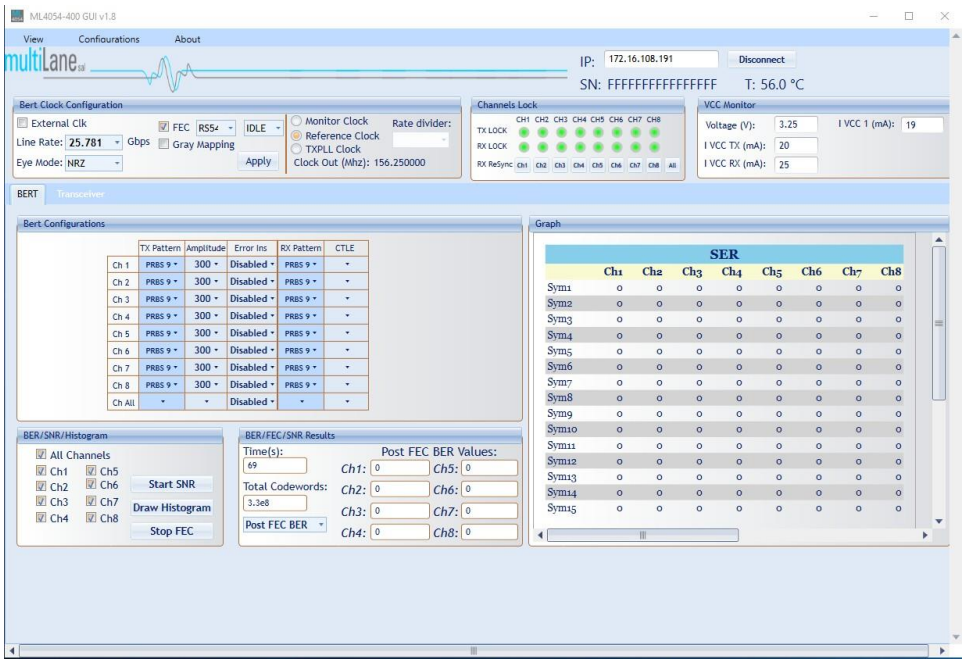


Figure 42: RX lock status updated

User can detect channel by channel the 3 FEC measurements: Post FEC BER, corrected codewords and uncorrected codewords. Based on the selection, while FEC is running, values in the display boxes will be updated.

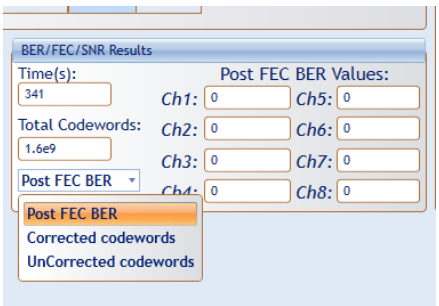


Figure 43: FEC measurements

For SER display, user can switch between the 3 supported display formats.

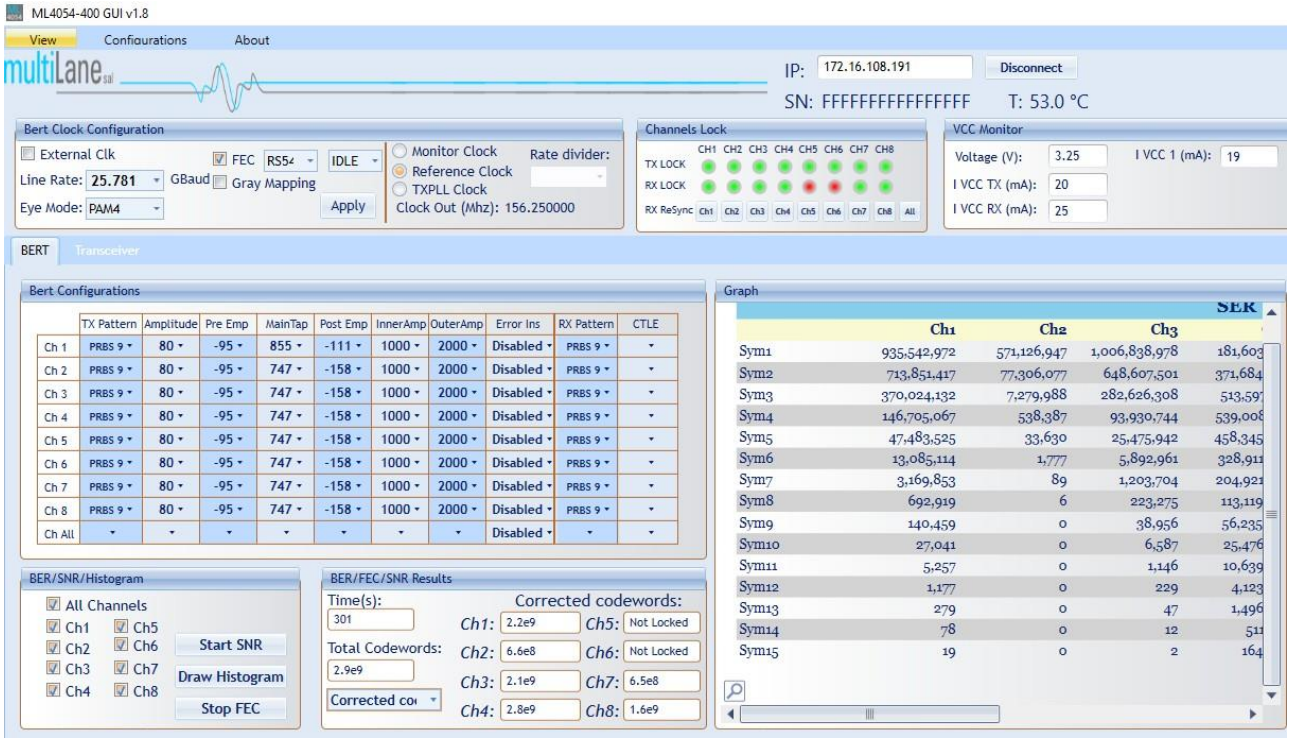


Figure 44: SER measurement results

14.5 Transceiver Tab

To read and control the transceiver settings the user should select the transceiver tab.

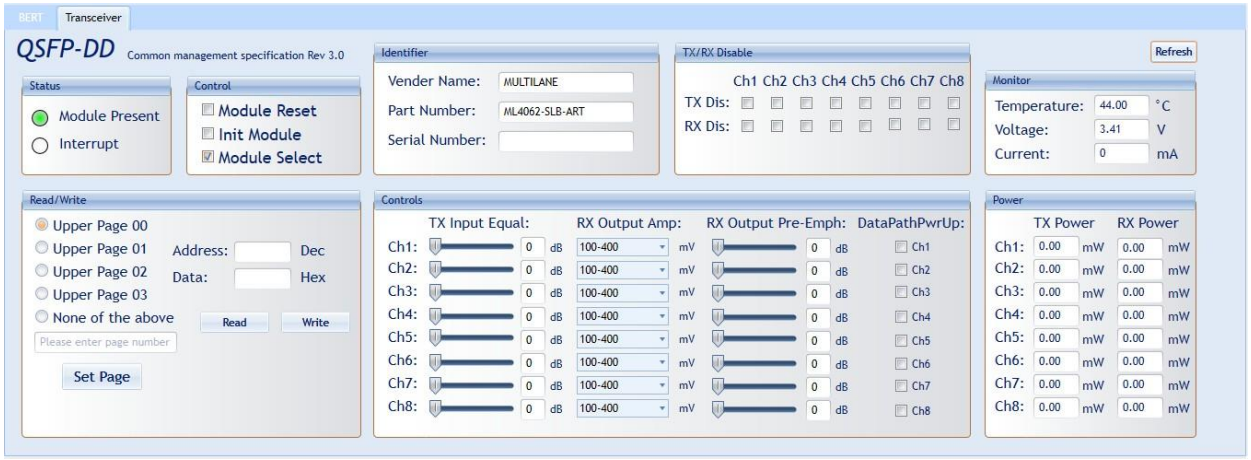


Figure 45: transceiver tab

The vender name, part number and serial number are automatically detected.

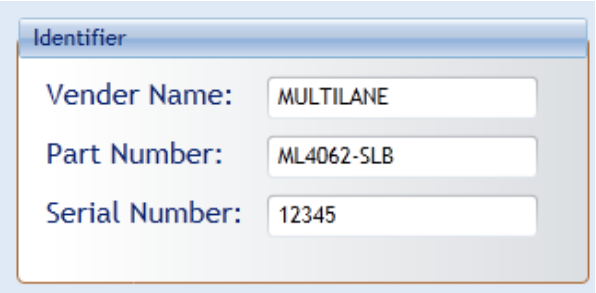
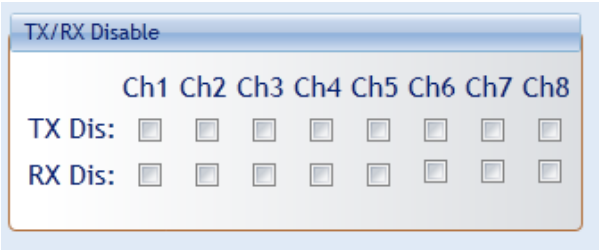


Figure 46: Module's identification

The control fields allow the host to dynamically change the behavior of the device.



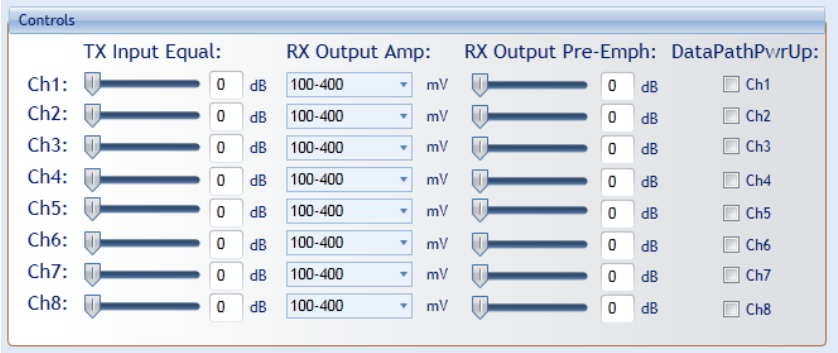


Figure 47: control tabs

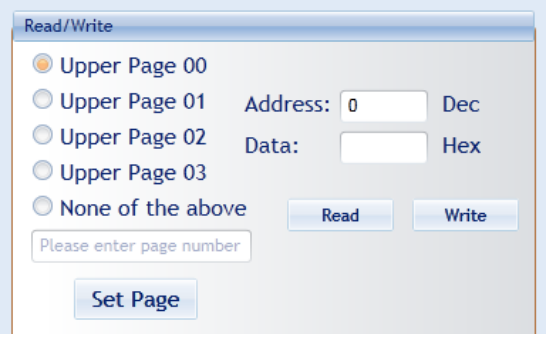


Figure 48: I2C Read/ Write

Hardware control signals (LPMODE, RESET_L, and MODSEL_L) can be controlled from this tab. The user can also get the state of INT_L and MODPRS_L signals.

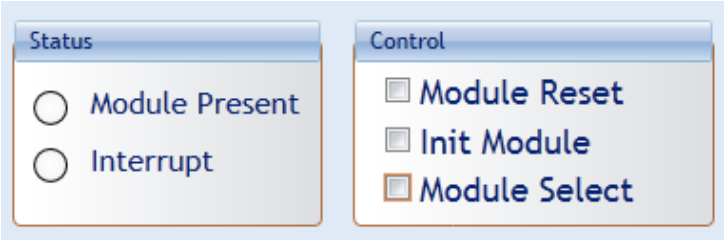


Figure 49: Control signals

15. IP changer tool

If the user needs to change the IP of the board, the link represented below, has all the tools needed. (Software and user guide).
https://multilaneinc.com/berts-gui/

Figure 50: IP changer GUI and User Guide

Figure51: Ethernet Configuration Software

16. Revision History

Revision number	Date	Description
1.0	11-20-2018	▪ Document created
1.1	11-21-2018	▪ Eye captures updated in paragraph 14.3
1.2	2-5-2019	▪ Block Diagrams updated in paragraph 4 ▪ Clock configuration updated in paragraph 7 ▪ 7 taps FIR description added in paragraph 8 and 14.3 ▪ SNR Low rate supported in fw above rev 1.8 ▪ Screenshots related to the 7 tap feature added to the user manual section

17. References

- QSFP-DD HARDWARE SPECIFICATION FOR QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER – REV 4.0
  http://www.qsfp-dd.com/wp-content/uploads/2018/09/QSFP-DD-Hardware-rev4p0-9-12-18-clean

- Rev1.12: Specification for OSFP Octal Small Form Factor Pluggable Module

  https://osfpmsa.org/assets/pdf/OSFP_Module_Specification_Rev1.12.pdf

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