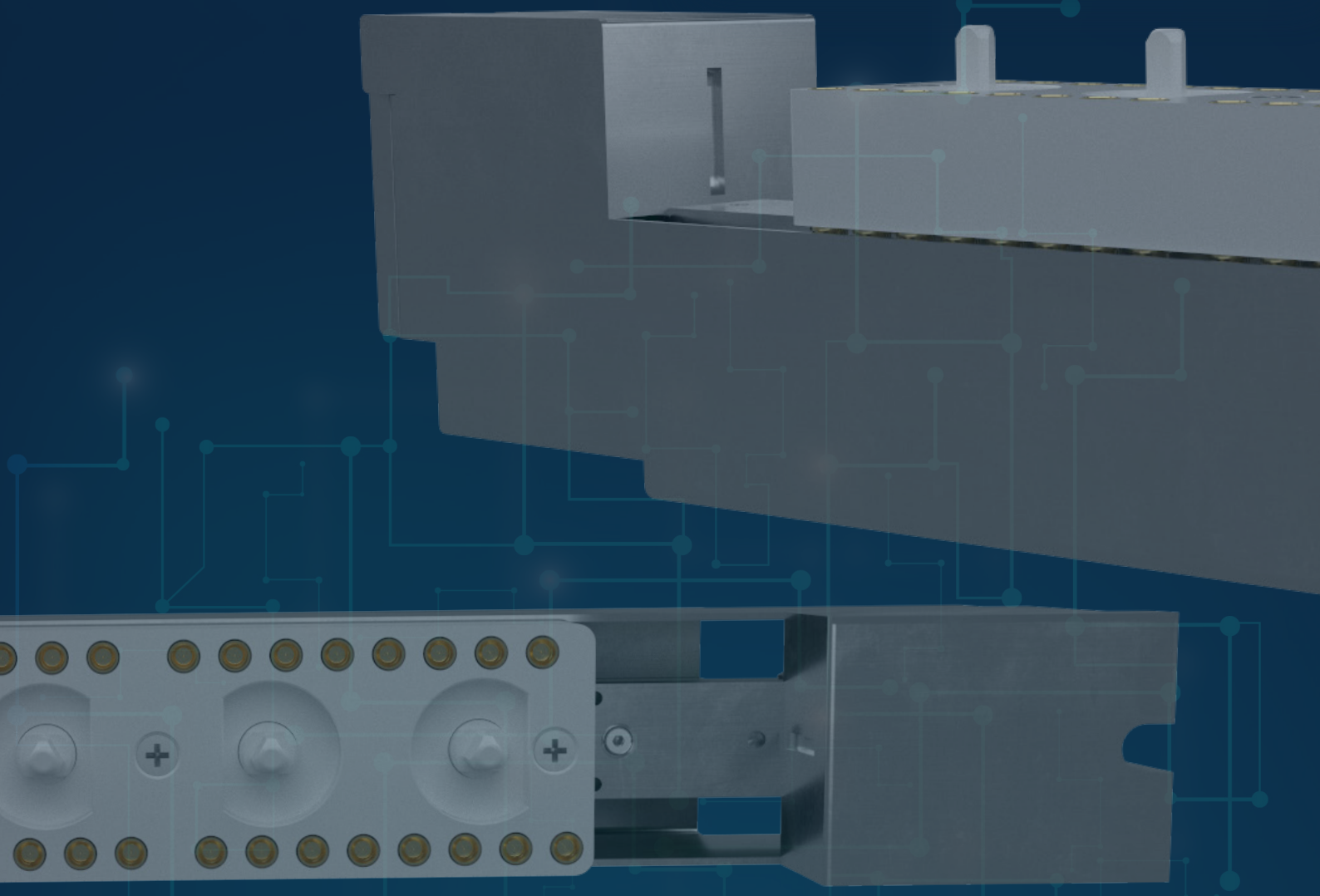
multiLane

V93000 HSIO

High-Speed Solution

Up to 48 bidirectional differential lane count | BERT and DSO, Source/Measure up to 224Gbps | NRZ and PAM4 | AWG with 96 GSa/s Fs | SmarTest API's | V93000 production ready | Loadboard accessories



Summary

Advantest and MultiLane offer a single platform solution which leverages the best capabilities and qualities of both companies. MultiLane high-speed BERT, scope DSO, and arbitrary waveform generator AWG high-speed instruments are fully integrated into Advantest's V93000 ATE tester, expanding digital and analog semiconductor IC characterization, validation and production testing capabilities. The BERT/DSO/AWG instruments provide testing capabilities of up to 48 differential lanes at up to 224 Gbps (PAM4) and 70 GHz bandwidth. V93000 Smartest software and hard docking solutions are already deployed worldwide, with proven reliable results in production environments.

This unique V93000 turnkey solution enables testing of packaged silicon as well as wafer high-speed I/O, and other active and passive high-speed devices. Testing is accomplished at the PHY level for Ethernet, USB 3/4, PCIe 5/6 and other high-speed serial I/O port types.

In addition, MultiLane offers ATE-related services including DUT load board design, and signal integrity simulation.

Key Features and Benefits

Key Features
- Up to 48 synchronized lane testing
- NRZ & PAM4 signals
- Blindmate RF cable connection
- V93000 Smartest Software API's
- Multisite ready software
- Direct Docking
- At-Speed Wafer sort testing
- At-Speed Package testing
- Easy movement of capabilities between bench and ATE
- complete set of APIs and multiple SmarTest sample code to speed up integration

Key Benefits
- High-speed interface testing
- Complementary testing capabilities to the V93000 test platform
- BERTs and SCOPEs compensate for cable and DUT board traces
- SmarTest tools help speed test program development and multisite deployment
- Advantest docking allows quick and reliable interfacing to a wide variety of device handlers and wafer probers

IC Package Testing | Final Test

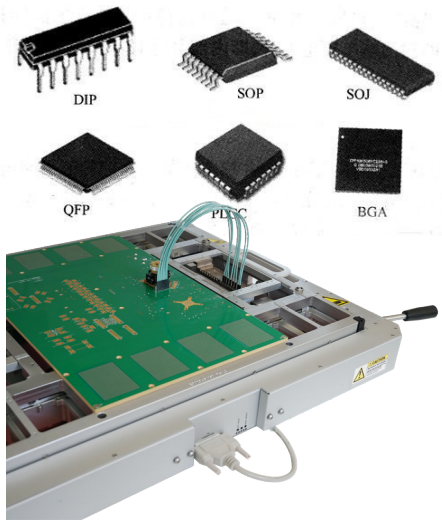
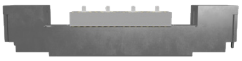


Figure 3: package testing

Wafer-Level Testing

Figure 4: wafer-level testing

Available Instruments

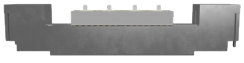


AT4080

4-lane, 64 GBaud AWG&BERT cassette

AT4025

4-channel, 35 GHz bandwidth digital sampling oscilloscope cassette



AT4039E

4-lane, 112 Gbps (56GBaud) BERT cassette

OT4039F

4-lane, 224 Gbps (112GBaud) BERT cassette

OT4025-70GHz

4-channel, 70 GHz bandwidth digital sampling oscilloscope cassette

EXA Scale MultiLane Extension

The OT93000 is designed for wafer sorting and final testing on the EXA-Scale Machine, compatible with CX, SX, and LX test heads.

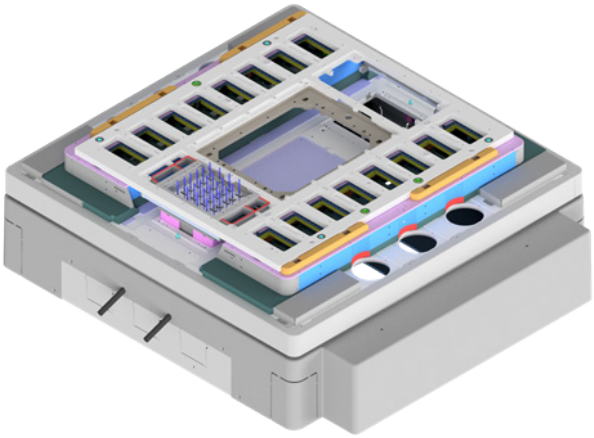


Figure 13: OT93000 system

Key Features

- Channel Density: Supports up to 48 channels with all 6 cassettes fully populated.
- Cooling and Power: Cassette instruments are water-cooled, powered by an external +12V supply, and communicate via Ethernet.
- MultiLane Cassettes: Accommodates up to 6 cassettes, each housing up to two high-speed MultiLane Instruments.

Figure 14: OT Cassette

The OT6000 backplane delivers power, communication, and clock signals to OT instruments, requiring a 12V, 15A power supply and featuring clock cabling, UART and firmware upgrade interfaces, Ethernet connectivity, and water intake for cooling.

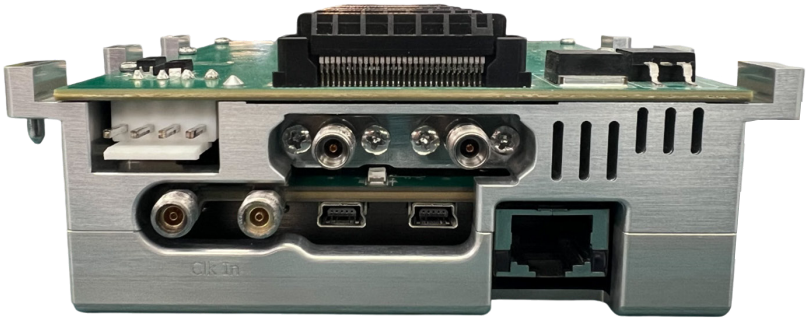


Figure 15: OT6000 Backplane

OT4025-70 GHz DSO Specs

4-lane DSO

Key Features

- Up to 100 MHz sampling rate
- Fast pattern capture and DSP thanks to an FPGA-based architecture
- An extensive library of built-in DSP filters such as Bessel-Thomson, CTLE, DFE, FFE, de-embedding and component emulation, all available free of charge in the standard GUI.
- User-writable calibration constants Can be calibrated up to the DUT to include losses of test fixtures and cables

Electrical Specifications

- Data format support: NRZ and PAM4
- Input Swing Max: 1200 mVpp
- Rise/Fall Time: 7 ps
- Vertical resolution: 14 bits
- Electrical channel bandwidth: 70 GHz

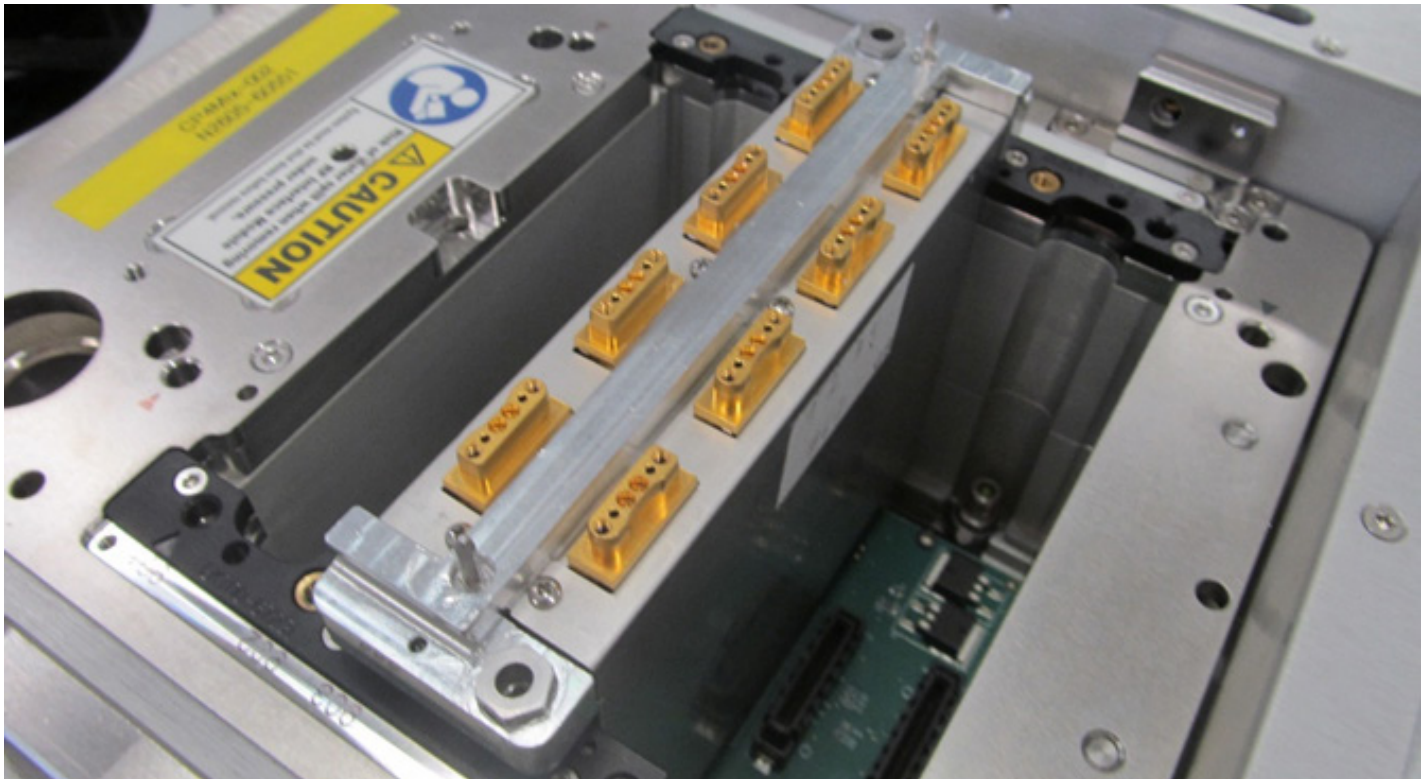


Figure 18: OT4025F DSO mounted is a system for wafer sort testing

OT4039F & AT4039E Bert Specs

4-lane BERT 112GBd/ 56GBd PAM4/NRZ

	4-Lane BERT 112 GBd PAM4/NRZ (OT4039FN)	4-Lane BERT 56 GBd PAM4/NRZ (AT4039E)
PPG Features	High-speed clock out to 7 GHz	High-speed clock out to 7 GHz
	Gray coding, polarity inversion	Real FEC and Gray coding
	PRBS7, 9, 13, 15 23, 31, 58	PRBS7, 9, 13, 15, 23, 31, 58
	PRBS13Q, 15Q, 31Q	PRBS13Q, 31Q
	Up to 1600 mVppd voltage swing	Up to 800 mVppd voltage swing
	Patterns are generated algorithmically	Patterns are generated algorithmically
	Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed	Patterns are generated algorithmically
ED Features	FFE Equalizers with reflection cancellation and DFE	FFE Equalizers with reflection cancellation and DFE
	PAM4 eye balance tuning	PAM4 eye balance tuning
	Eye contour and PAM level histogram	Eye contour and PAM level histogram
	PRBS7, 9, 13, 15, 23 & 31 checker	PRBS7, 9, 13, 15, 23 & 31 checker
	Automatic PRBS detection	Automatic PRBS detection
	Clock-data recover	Clock-data recover
	BER counters	BER counters

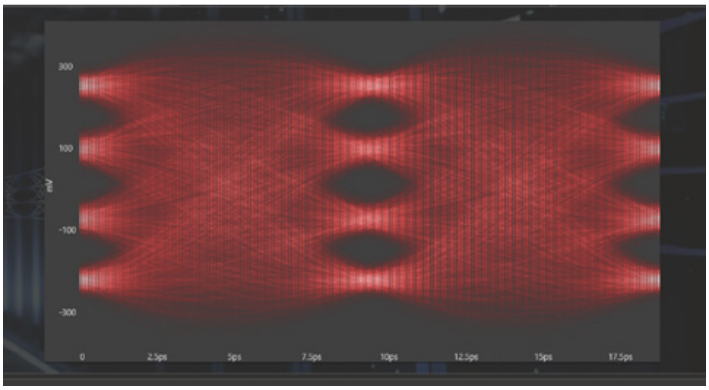


Figure 16: PAM4 Signal at 224G

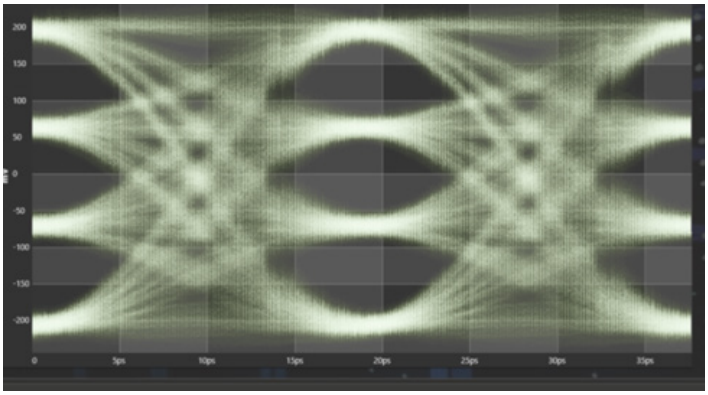


Figure 17: PAM4 Signal at 53G PRBS13Q

V93000 HSIO System Overview

The BERTs, DSOs, and AWGs are located directly under the load board, in the cavity of the test head extender called the Twinning Frame. Due to this proximity to the load board, the signal path from MultiLane instruments to the DUT is extremely short. This signi icantly enhances signal integrity and test accuracy.

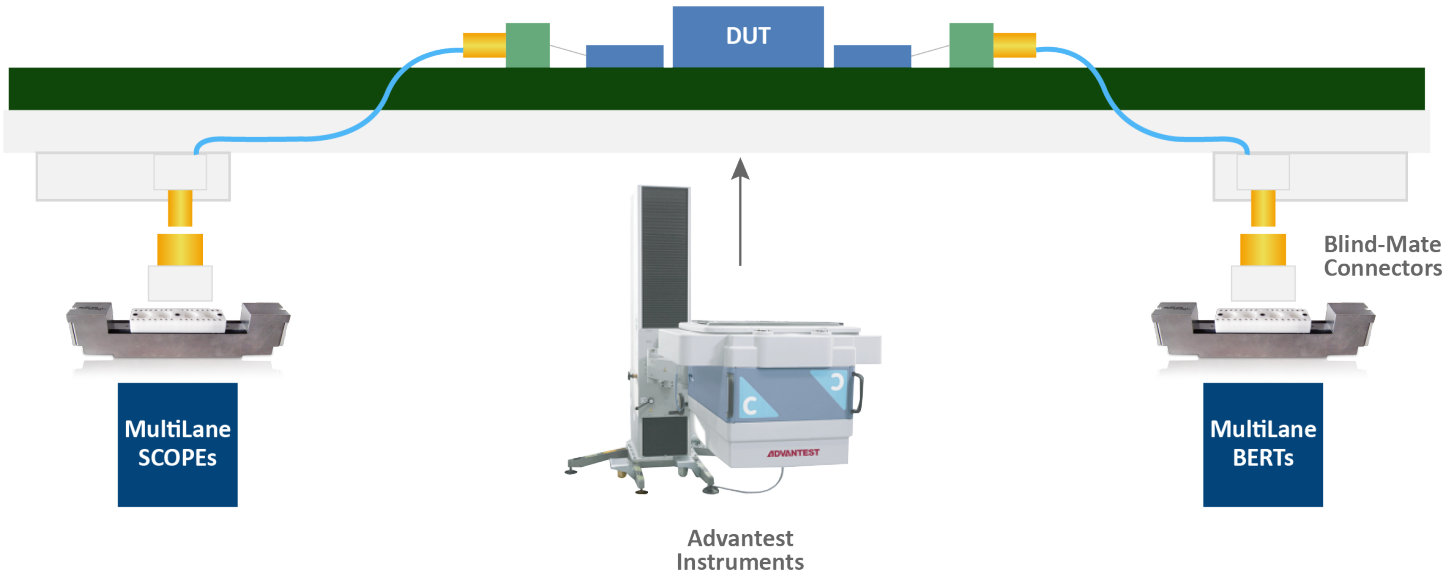
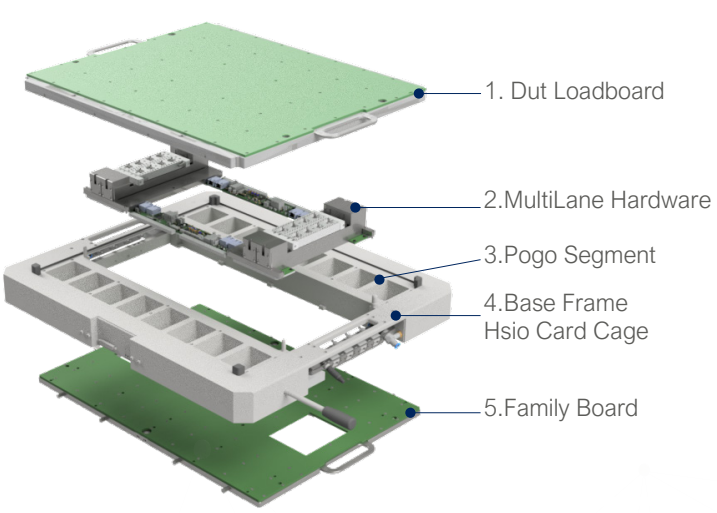


Figure 1: Overview of the V93000 HSIO System



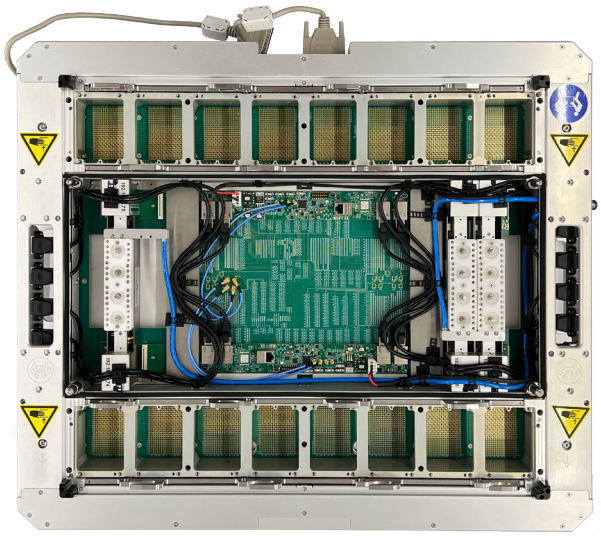


Figure 2: HSIO MultiLane cassettes mounted inside a twinning frame.

AT4080 (Arbitrary Waveform Generator) Specs

4-lane BERT-PPG PAM4/NRZ & AWG 64 GBdn.

Key Features

- The wide range of bitrate coverage allows PHY testing of Ethernet, PCIe Gen 4/5/6, USB, Automotive A-Phy & in-Vehicle Communication & others
- Independent control of inner eye levels
- Ability to tune the bit rate in very fine step to facilitate finding locking margin
- Library of pre-defined waveforms
- Ability to generate custom modulation like PAM7, PAM9, etc. in AWG mode

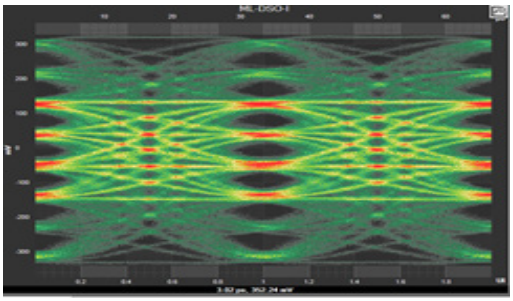
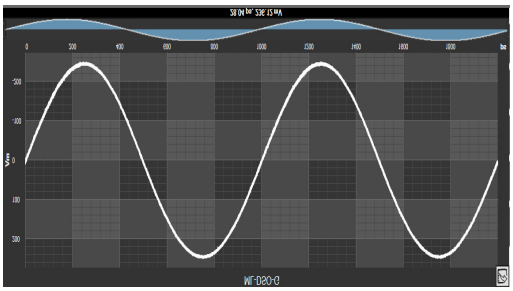


Figure 5: PAM8 Signal at 53G

PPG Features

- Bit Rates: 25 – 64 GBd
- Modulation: NRZ and PAM4
- Tx Maximum PRBS Amplitude at 26G: 750 mVppd (350 mVppd in calibration mode)
- Tx Maximum PRBS Amplitude at 53G: 500 mVppd (300 mVppd in calibration mode)
- Patterns: PRBS7/9/11/15/20/23/29/31/35/39/41/47
- TX Amplitude Adjustment Steps of 1 mV
- TX Equalization: FFE 3 taps or 7 taps



AWG Features

- Tx Maximum Amplitude (Sine wave): 1050 mVppd
- Bit Rates: 1 – 64 GBd
- Vertical Resolution: 8 bits
- Modulation: User-defined
- Pre-programmed Waveforms: PRBS 7, PRBS 9, Square wave, triangular Wave, sine wave, multi-tone, Linear chirp, log chirp, sawtooth, exponential rise, exponential decay, Sinc, Lorentz, Surge, Damped Oscillation, Stairs, Serial Data, half-sine, Distorted sinewave and Gaussian.
- Memory Depth: 33.6 kSa per channel
- Jitter Injection & other impairments available

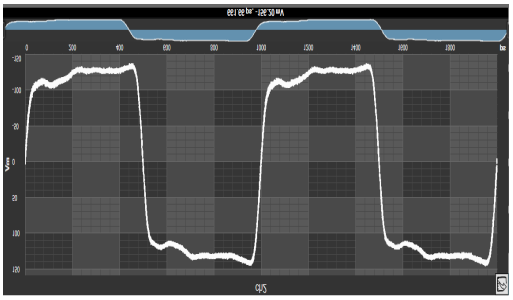
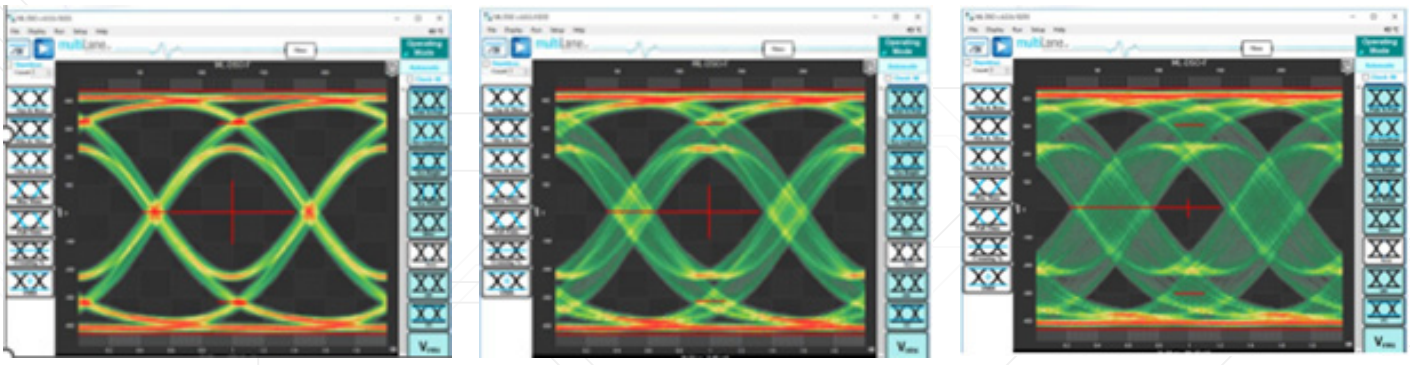


Figure 6 :Predefined waveforms



10ps 30ps 60ps

Figure 7: PRBS11-Signal generated with SJ insertion at 2MHZ and ISI at 6db

AT4025 DSO Specs

4-lane DSO

Key Features

- Up to 100 MHz sampling rate
- Fast pattern capture and DSP thanks to an FPGA-based architecture
- An extensive library of built-in DSP filters such as Bessel-Thomson, CTLE, DFE, FFE, de-embedding and component emulation, all available free of charge in the standard GUI.
- User-writable calibration constants Can be calibrated up to the DUT to include losses of test fixtures and cables

Electrical Specifications

- Data format support: NRZ and PAM4
- Input Swing Max: 1400 mVpp
- Rise/Fall Time: 9.5 ps
- Vertical resolution: 16 bits
- Electrical channel bandwidth: 35 GHz

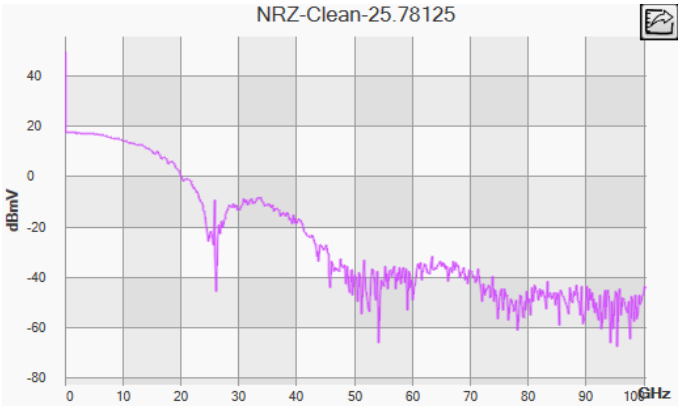


Figure 8:Measuring Total Harmonic Distortion

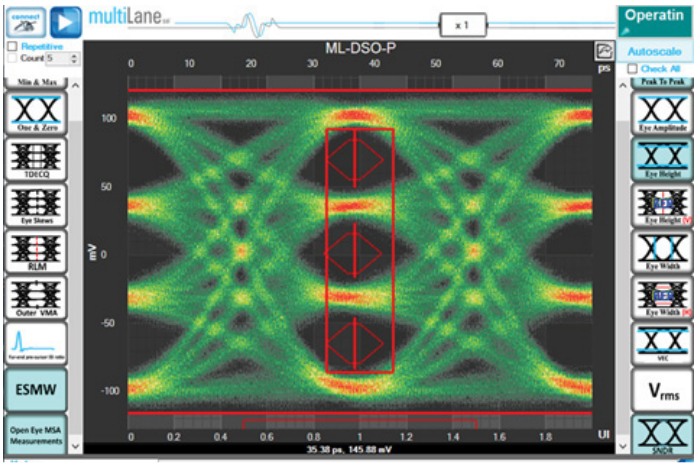


Figure 9: PAM4 Eye Measurements

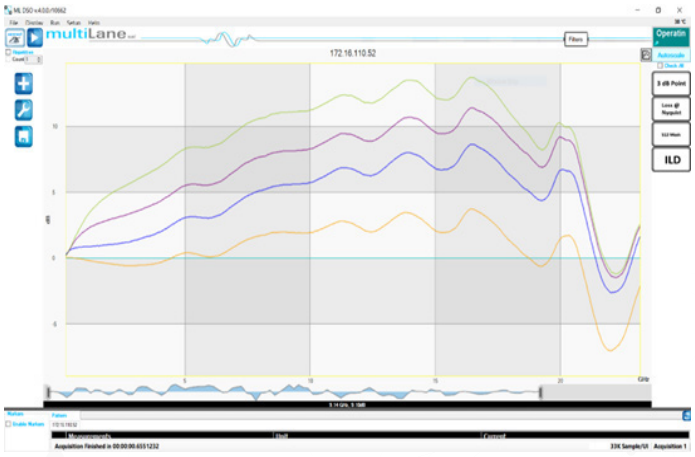


Figure 10: Gain and peaking measurements for PCIe express Gen6 re-driver.

Software Integration| SMT8

- Multilane Shared Libraries for RHEL5, RHEL7 and RHEL7.9 SMT8
- SmartRDI-like Implementation
- Supports Multi-site Testing
- SmarTest sample code available
- High throughput features
- Time-consuming computations can be done in background using SmartCalc
- Co-developed with Advantest
- Eclipse fully supported

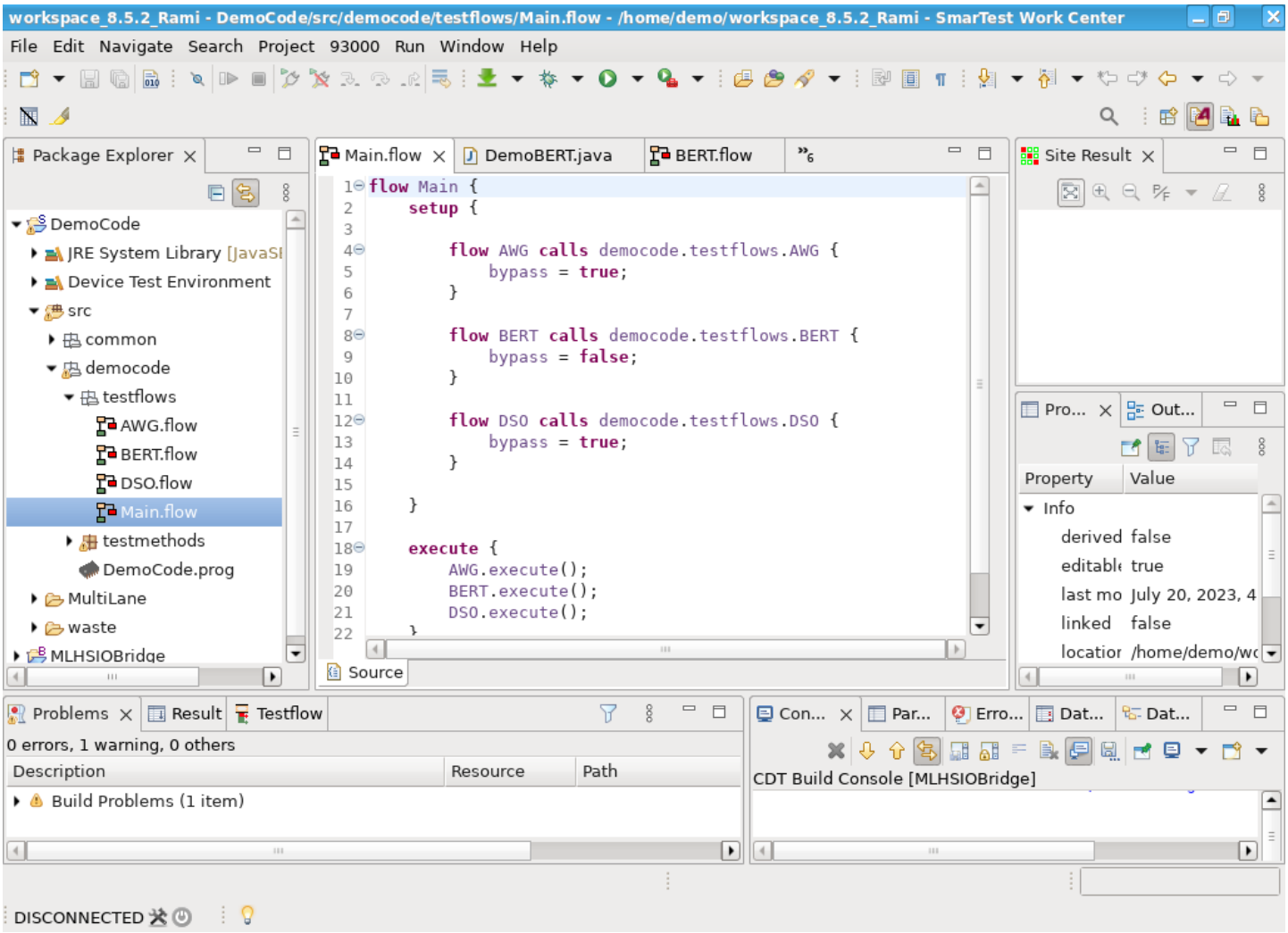


Figure 11: Smart Test Integration

V93000 Control

- Advantest Smartest 7.x and 8.x software API's
- Advantest Multisite software methodology
- Full use of all Advantest Smartest software features such as debugging and datalogging
- High throughput multithreaded DSP routines Windows based control
- Alternative laptop Ethernet control path into MultiLane instruments using MultiLane GUI window software

Windows based control

- Alternative laptop Ethernet control path into MultiLane instruments using MultiLane GUI window software

AT-93000UBOX

- AT93000-UBOX: centralized utility box for Power, Compressed Dry Air (CDA) and Ethernet Hub.
- Inputs: facility power, CDA air and an Ethernet connection from the V93000 workstation.
- Outputs: 12V power for MultiLane high-speed instruments, regulated air for instrument cooling, and ethernet cables for instrument communication.

Figure 12: Utility BOX

Ordering Information

Details	Product Number
4-channel 50 GHz Bandwidth Digital Sampling Oscilloscope. ½ cassette	AT4025
4-channel 70 GHz Bandwidth Digital Sampling Oscilloscope. ½ cassette	OT4025-70 GHz
4-lane 112 Gbps (56 GBaud PAM4/NRZ) BERT. ½-cassette	AT4039E
4-Lane 224 Gbps (112 GBd PAM4/NRZ) BERT. ½-cassette	OT4039FN
4-Lane, 64GBaud AWG & BERT PAM4/NRZ	AT4080
Twinning Frame infrastructure	Contact MultiLane
Package Test and Wafer Probe Test Loadboard Accessories	Contact MultiLane
Specialized high-speed cable assemblies	Contact MultiLane
ATE-related application services	Contact MultiLane

MWTP ATE head mounting system

The BERTs, DSOs, and AWGs are located directly under the load board, in the cavity of the test head extender called the Twinning Frame. Due to this proximity to the load board, the signal path from MultiLane instruments to the DUT is extremely short. This significantly enhances signal integrity and test accuracy.

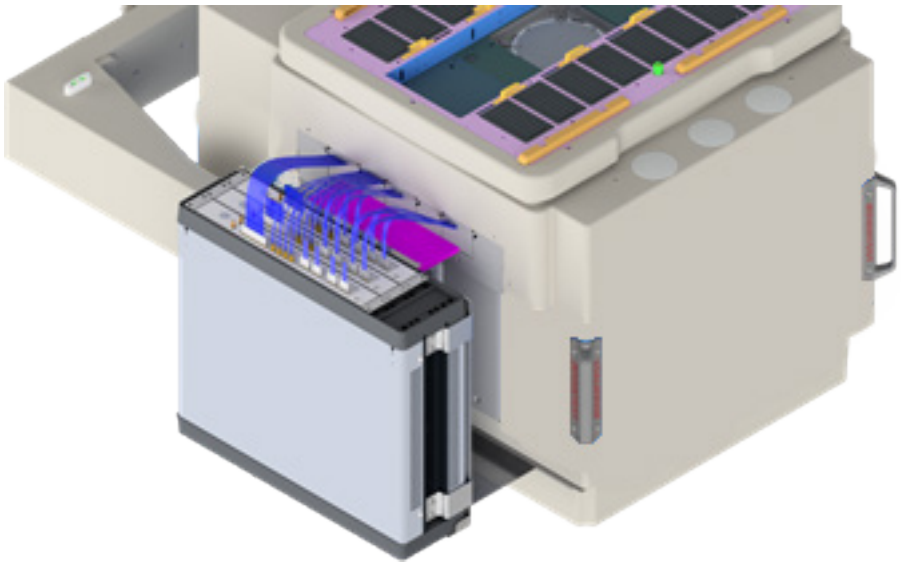


Figure 19: OT93000 system

Key Features

- Compact & optimized density
- Versatile & simplified setup for new products
- Cost-effective solution
- Enhances existing ATE systems
- Bridges the gap between characterization and production
- Tester-agnostic ATE solution with 16 to 256 ultra-wideband pins
- Reduced test time
- Super slim 1U rack-and-stack testing solution
- Models & options chassis system with user-selectable configurations
- Supports any mix of BERTs, scopes, AWGs, TDRs, protocol testers, and AWGN
- Modular & customizable connectivity
- Interactive library of measurements and automated data collection
- Test head mountable
- Convection-cooled for bench usage
- Modular design
- Ultra low-profile

Figure 20: MultiWave Test Platform

multiLane

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