multiLane

Stress Testing Innovations for High Speed I/O

A New Bar for SerDes Margin Testing

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Stress Testing Across SerDes Generations

The accelerated pace of high-speed interconnect innovation has meant that every new technology node sees a paradigm shift in testing methodologies. 112Gbps/lane PAM4 signaling – widely adopted in ethernet connectivity today – has increased sensitivity to jitter and noise and requires very rigorous validation testing. Faster data rates naturally lead to shrinking performance margins. Cloud and AI/ML applications are actively driving all segments of a network link to be comprehensively stress tested in development and manufacturing environments alike.

The industry is in the process of refocusing on a well-rounded validation cycle, with jitter and noise tolerance testing serving as critical components to receiver and system testing, providing multi-dimensional insights into 112Gbps/lane technologies crucial for rapid time-to-market.

MultiLane's position in this new testing landscape is clear: set a new standard for scalable stress testing technology with a full suite of jitter and noise injection tools. MultiLane solutions meet and substantially exceed the impairment thresholds defined by industry standards publications to determine if a Device Under Test (DUT) is robust enough to function reliably over a range of operating conditions with adequate margin.

This white paper will outline the set of test capabilities that include design validation, component characterization, and system-level sensitivity and stress tolerance. 800 Gigabit communication links can now be reliably and cost-effectively validated with MultiLane stress injection instruments.

Key Takeaways:

- Jitter and noise testing now crucial at 112Gbps/lane
- MultiLane aims to reset the standard in scalable jitter/noise testing tools

Jitter and Noise: Causes and Classifications

Jitter and noise refer to specific kinds of signal disruption which degrade the quality and integrity of a serial link. Jitter is a measure of uncertainty in horizontal signal timing, offsetting it from its nominal value, while noise distorts vertical signal amplitude.

Jitter and noise are not mutually exclusive and can occur simultaneously on a single link.

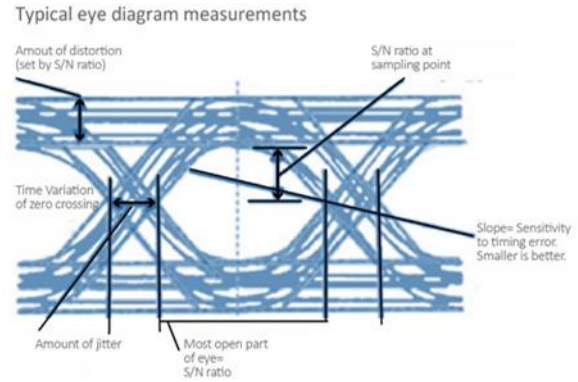


Figure 1: Jitter and noise effect on eye shape

Sources of Jitter and Noise

Intrinsic Sources

Some jitter and noise sources – known as intrinsic sources – are inherent to the physical properties of the electrons residing in semiconductor devices. These are most often the result of fluctuations caused by a device's thermal characteristics or random current variations. While being a characteristic of all data rates, the increased sensitivity of 800G+ makes new devices much more prone to interference from these sources.

Non-Intrinsic Sources

Non-intrinsic sources of jitter and noise are related to the flaws in a device's design: whether an offset variation in a signal's timing, or non-ideal characteristics in a channel's frequency response. Impairments caused by non-intrinsic, deterministic origins can be more easily mitigated than intrinsic sources, if not made negligible altogether.

Crosstalk

In the tightly packed real-estate of High-Speed Input/Output (HSIO) interfaces, energy from one signal transition can leak into neighboring or adjacent channels causing the signal level in those channels to fluctuate. Crosstalk is most prevalent in copper communications, incurring amplitude noise in the transmitting signal and consequently timing jitter through the slew rate[1] conversion, which degrades overall system performance.

Key Takeaways:

- Intrinsic jitter and noise are inherent to a system
- Often caused by a design flaw
- Crosstalk occurs when signal leaks into adjacent channels

[1] Slew Rate: The ability to adjust the rate of signal change, controlling the speed of bit transition between levels. Rapid signal change at 112Gbps/lane necessitates an understanding of the effect of high speed on the system. Predicting slew rate is a critical factor in system design to avoid reflection and overshoot/undershoot effects, further control the effect of crosstalk, and predict DUT receiver Rx reaction to different slew rates.

Jitter Types

The total jitter (TJ) of a given system is comprised of random jitter (RJ) and deterministic jitter (DJ) to differentiate between impairments caused by compounding small noise effects (RJ) and those whose elements can individually be traced to specific properties of the DUT (DJ).

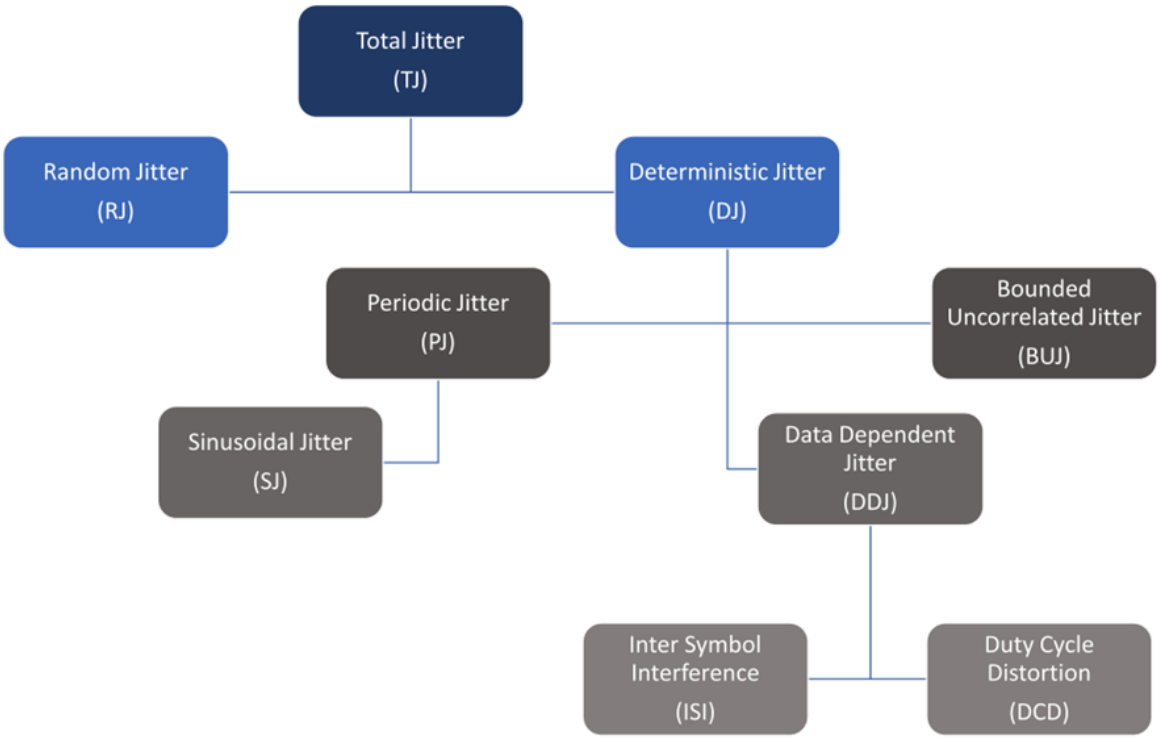
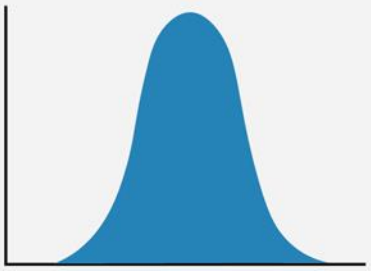
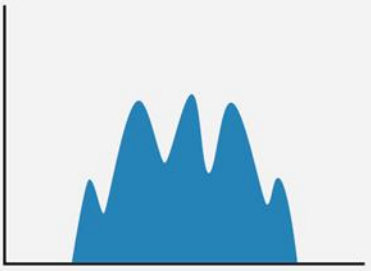
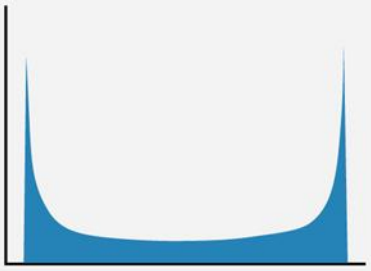


Figure 2: Breakdown of jitter components

The jitter types most frequently applied in stress testing are illustrated in the table below:

Table 1: Frequently applied jitter types

Jitter Type	Definition	Histogram
Random Jitter (RJ)	Jitter attributed by small noise elements such as thermal noise of the semiconductor or microscopic variations in the resistance and impedance of circuit traces. Unlike its deterministic counterpart, RJ follows an unbounded distribution.	
Bounded Uncorrelated Jitter (BUJ)	BUJ encompasses the effects of crosstalk. Contrary to RJ, this high probability jitter is bounded and deterministic, even if it encompasses noise with root causes outside of the designer's control.	
Sinusoidal Jitter (SJ)	SJ represents a signal timing error for a specific frequency. The IEEE Std 802.3-2018, IEEE Standard for Ethernet (Section Four) defines SJ as a critical parameter for stressed eye calibration following a magnitude ranging between 40 kHz and 10 times the Loop Bandwidth.	

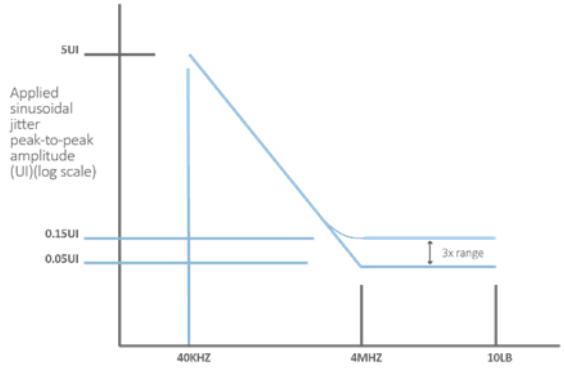
Key Takeaways:

- Random Jitter accounts for small noise elements
- Forms of Deterministic Jitter critical for testing:
  - Sinusoidal Jitter
  - Bounded Uncorrelated Jitter

Jitter Tolerance Testing

Jitter tolerance testing (JTOL), also known as stressed input testing, determines the robustness of a receiver in the face of signal impairments which typically occur in the network path. Jitter can be effectively classified into unique components (see figure 2), each a result of a specific phenomenon and unique DUT properties.

The JTOL procedure entails injecting a precise combination of these impairments through a DUT, enabling accurate system characterization by determining the precise impact of these components on transmission quality by measuring the resulting BER.



Frequency range	Sinusoidal jitter (UI pk to pk)
f < 40kHz	NA
40 kHz < f ≤ 4MHz	2 x10^6 / f + S – 0.05[a]
4 MHz < f < 10 LB[b]	0.05 ≤ S ≤ 0.15[a]

[a]S is the magnitude of sine jitter actually used in the calibration of the stressed eye per the methods of 52.9.9.3.
[b]LB = Loop Bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

Figure 3: IEEE 802.3 SJ Injection Mask

Some tests require different jitter injection types: the IEEE 802.3ck – 120G.3.4.3.2 Module Stressed Input Test Calibration, for example, calls for a combination of sinusoidal, random, and bound uncorrelated jitter injection.

Random and bounded uncorrelated jitter are requirements for this compliance test because they produce a signal profile which approximates JRMS (max) and J4u (max), complying with the even-odd jitter (max) specification in Table 120F–1. These are initial jitter values that will be modified as the stress injection test progresses.

The parameters after calibration shall follow Table 120G–10—Module stressed input parameters. As for the SJ injection, it shall follow IEEE 802.3ck Table 162–16—Receiver jitter tolerance parameters.

Table 2: IEEE 802.3ck Table 120F–1—Transmitter electrical characteristics at TP0v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
Differential peak-to-peak output voltage[b] (max) Transmitter disabled Transmitter enabled	93.8.1.3	35 1200	mV mV
Common-mode voltage[b] (max)	93.8.1.3	1	V
Common-mode voltage[b] (min)	93.8.1.3	0.2	V
Signal to AC common-mode noise ratio, *SCMR* (min)	163.9.2.7	16	dB
Difference effective return loss, *dERL* (min)	120F.3.1.1	-3	dB
Common-mode to common-mode return loss, *RLcc* (min)	162.9.3.6	2	dB
Difference steady-state voltage, dv_f (min)	163.9.2.4	0	V
Difference linear fit pulse peak ratio, dR_{peak} (min)	163A.3.2.1	0	-
Level separation mismatch ratio, R_{LM} (min)	120D.3.1.2	0.95	-
Output waveform[c] absolute value of step size for all taps (min) absolute value of step size for all taps (max) value at min state for c(–3) (max) value at max state for c(–3) (min) value at min state for c(–2) (max) value at max state for c(–2) (min) value at min state for c(–1) (max) value at max state for c(–1) (min) value at min state for c(0) (max) value at min state for c(1) (max) value at max state for c(1) (min)	162.9.3.1.4 162.9.3.1.4 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5 162.9.3.1.5	0.005 0.025 -0.05 0 0 0.1 -0.3 0 0.5 -0.1 0	- - - - - - - - - - - -
Signal-to-noise-and-distortion ratio, SNDR (min)	162.9.3.3	32.5	dB
Residual intersymbol interference, *ISI_RES* (max)	163.9.2.6	-31	dB
Output jitter J_{RMS} (max) J4u (max) Even-odd jitter (max)	120F.3.1.3 120F.3.1.3 120F.3.1.3	0.023 0.118 0.025	UI UI UI

[a]For a PMA in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the signaling rate presented to the input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMD, PMA, or FEC sublayers.
[b]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[c]The state of the transmit equalizer is controlled by management interface.

Table 3: IEEE 802.3ck Table 120G–10—Module stressed input parameters

Parameter	Value	Value
Pattern generator transition time (target)	9	ps
Applied peak-to-peak sinusoidal jitter	Table 162–16	-
Eye height (target)	10	mV
Vertical eye closure, VEC (min)	12	dB
Vertical eye closure, VEC (max)	12.5	dB
Crosstalk differential peak-to-peak voltage	845	mV
Crosstalk transition time	8.5	ps

Table 4: IEEE 802.3ck Table 162–16—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Units
Jitter frequency	0.04	1.333	4	12	0.40	MHz
Jitter amplitude	5	0.15	0.05	0.05	0.05	UI

Interference Tolerance Testing

Another fundamental stress characterization parameter is Interference Tolerance (ITOL). A DUT's reliability is measured by its ability to maintain a correct BER when subjected to elevated levels of signal distortion.

According to the Central Limit Theorem, the summation of random noise sources obeys a Gaussian distribution. As such, the IEEE Standard for Ethernet 802.3-2018 annex 93C paragraph 1 stipulates that Gaussian White Noise be synthesized via channel noise generators.

White noise itself can be likened to white light in that it is a random form of signal distortion characterized by a wide frequency spectrum with no dominating frequencies. Its primary characteristic is its uniform power spectral density across all frequencies and lack of any specific patterns or trends. This uniformity makes white noise particularly useful in high-speed testing as it can evaluate DUT performance across a wide spectrum of frequencies. The lack of a pattern in white noise also means that it can reveal design weaknesses or failure points that would not appear under more controlled conditions. White noise is therefore an essential factor in determining the robustness of a DUT, considering that it is particularly detrimental to data detection and processing.

Figure 5 shows the Noise Spectral Density requirement for this IEEE impairment.

The Crest factor describes the Gaussian nature of noise distribution and defines its quality. It is quantified by peak-to-peak amplitude over standard deviation with a target magnitude greater than 5 as per IEEE 802.3 Annex C documentation.

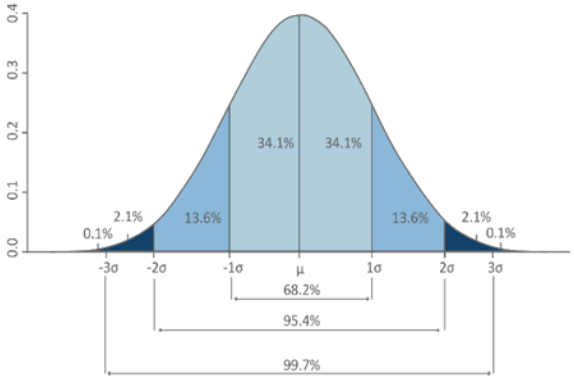


Figure 4: Gaussian Distribution

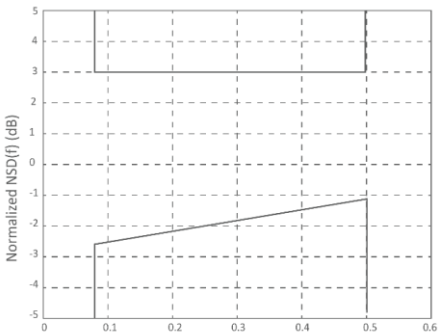


Figure 5: Spectral flatness per IEEE 802.3ck specs

Key Takeaways:

- White noise is essential to determining the robustness of a DUT
- The IEEE requires Gaussian White Noise be produced by channel noise generators
- The Crest Factor target magnitude must be greater than 5

Ratio of Level Mismatch Stress Test

Specific to PAM4 signaling – where multiple simultaneous eyes should ideally be equally spaced – the Ratio of Level Mismatch (RLM) measures how close the eye values are to each other when the inner/outer values are changed. RLM stress tests validate receiver tolerance to non-linearity in PAM4 Mode by giving the ability to skew the eye height on one eye to the other and measuring the RLM. The obtained value is compared to the IEEE 802.3 Transmitter Characteristics Value for Compliance Evaluation.

The below figure shows a PAM4 eye with varying eye levels.

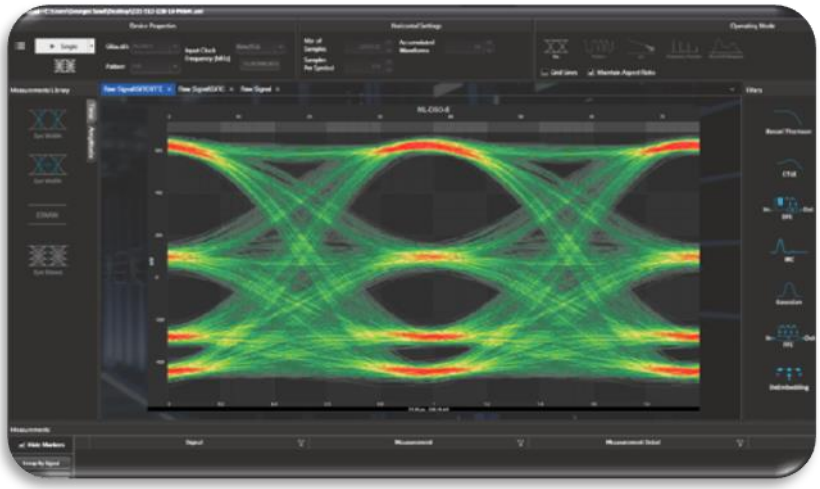


Figure 6: Adjusting different inner/outer eye levels

MultiLane Stress Testing Capabilities

Increased complexities of chip architectures have resulted in an ever-growing need for jitter and noise resilience for high-speed DUTs to be fully validated for network deployment. Widespread availability for jitter and noise tolerance testing is therefore essential. MultiLane offers turnkey solutions to ensure that DUTs can meet and exceed tolerance expectations.

Manual Jitter Testing

For manual jitter insertion, DUTs can be tested at line rate, with injected frequency modulation and phase modulation, additionally paired with RJ and BUJ, following the IEEE Standard Requirements. For SJ injection magnitudes, MultiLane capabilities exceed the IEEE requirements by up to three times, allowing for residual performance margin to be accurately quantified.

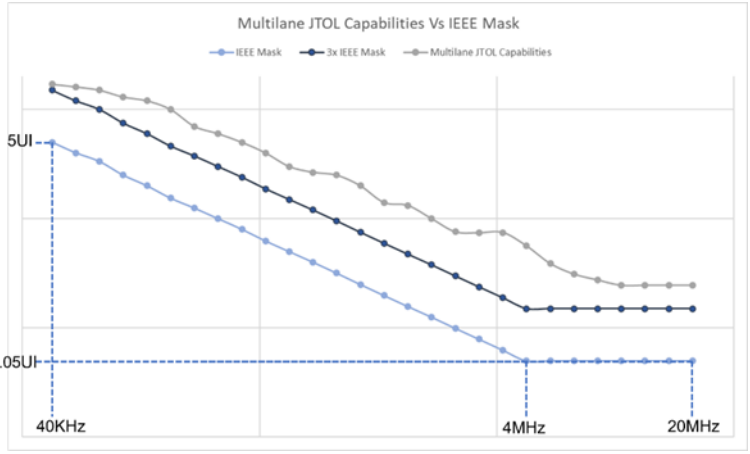


Figure 7: MultiLane SJ injection capabilities

Figure 8: MultiLane supported jitter types

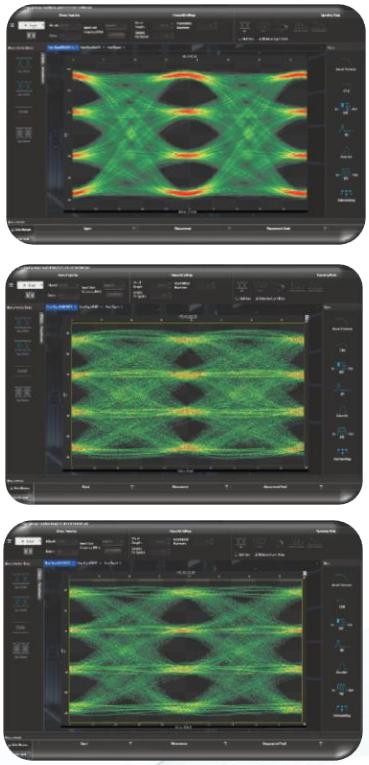


Figure 9: SJ effect on eye shape

Automated JTOL Testing

MultiLane provides automated solutions for both Single Frequency and IEEE JTOL through ThunderBERT. ThunderBERT allows users to verify results both during and after JTOL testing, with a pop-up table that can be displayed in table mode or by hovering the cursor over each test point in graph mode, and can export a CSV file with full test details of the JTOL test.

Single frequency JTOL

Single Frequency JTOL lets users select or input their requested frequency as well as SJ amplitude range, target BER and BER test time. JTOL results of the signal are displayed for comparison with the corresponding IEEE-defined frequency. A pass/fail assessment is issued after comparison to user-defined target BER. By isolating a single frequency and running the test over a range of jitter amplitudes, the DUT's breaking point can be identified rapidly. Using this feature, users are free to test their required frequency and amplitude range without the need for a standard reference, and can benefit from all monitoring, automation, and saving options.

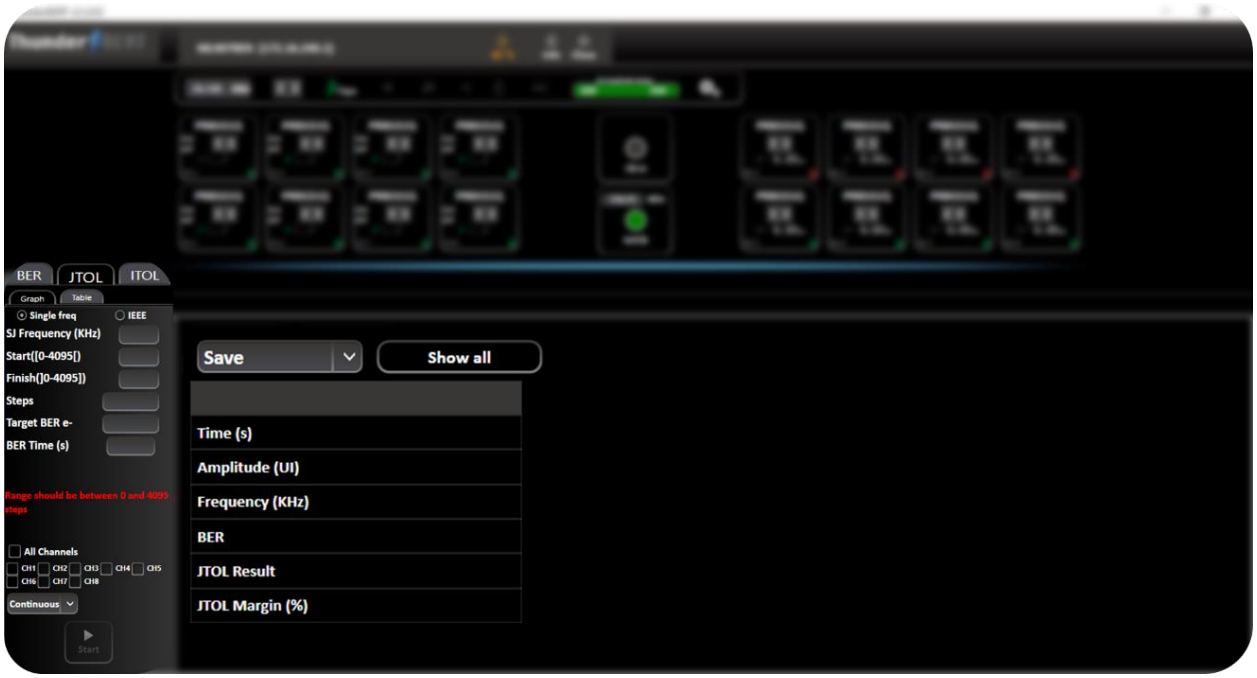


Figure 10: Single frequency JTOL control and results table

IEEE JTOL Testing

A substantial R&D time saver, the automated built-in JTOL guides users to select the IEEE Standard they wish to test their signal against – CAUI4, 400GAUI-8 and 800GAUI-8 – while defining the passing/target BER and BER test time per capture.

As with manual jitter measurements, actual JTOL performance data are displayed in comparison against the IEEE Mask. The resulting BER is compared with a previously selected target BER.

An automatic margin testing routine is also offered to determine the peak passing point (the largest jitter magnitude that yields a passing BER) as follows:

$$\text{Jitter Margin} = \frac{\text{Total inserted jitter} - \text{IEEE Mask}}{\text{Total inserted jitter}} \times 100$$

Figure 11: IEEE JTOL in graph mode

Figure 12: IEEE JTOL in table mode

ITOL Interference Tolerance Testing

MultiLane ITOL capability follows the specifications of the IEEE Standard for Ethernet (section 6, Annex 93C), which states that the noise shall be Gaussian white noise with a flat frequency response as per the Mask in the following figure and a Crest Factor greater than 5.

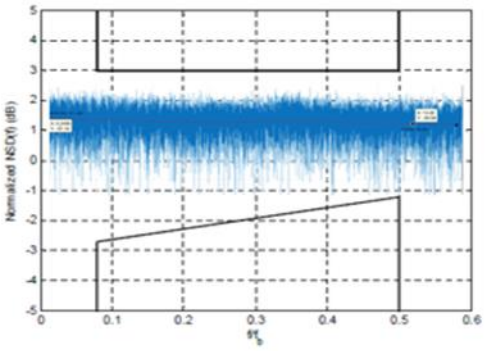
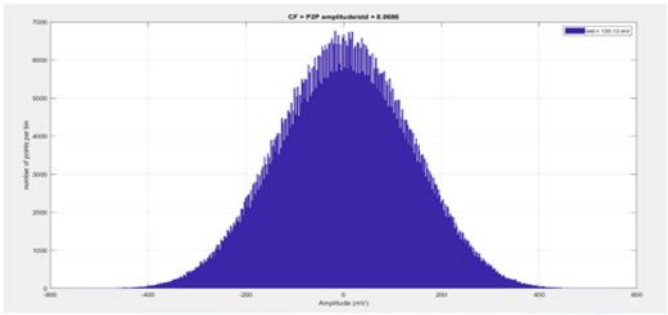


Figure 93C–1—Example NSD(f) constraint template

Noise Flatness



Crest Factor Measurement: Gaussian Noise

Figure 13: MultiLane random noise injection capabilities

ThunderBERT provides an automated ITOL test that compares BER at different selected amplitudes, then provides a pass/fail verdict with an option to save and export the result.

MultiLane supports calibrated random noise injection in mV-rms at each 2 adjacent channels independently. Users can control the noise amplitude slider and subsequently monitor the effect on both BER and eye shape.

Figure 14: Random noise calibrated slider

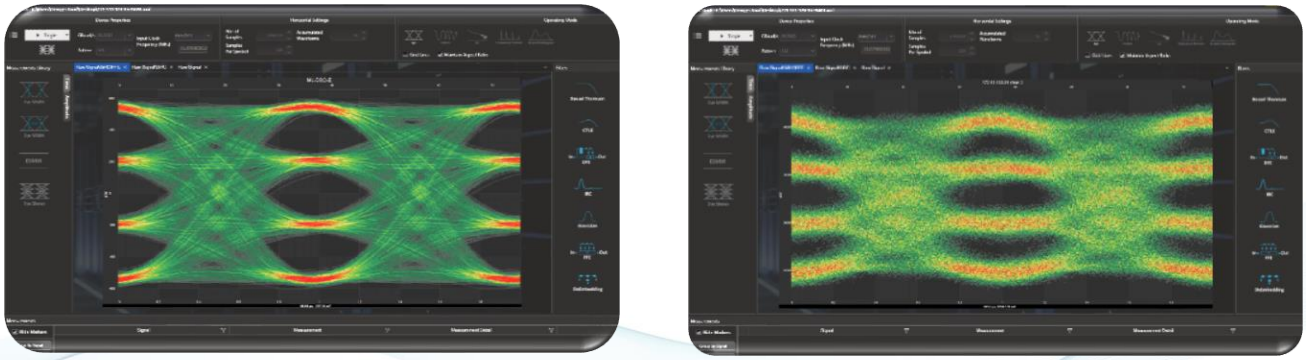


Figure 15: Noise effect on eye shape

Additional Features

RLM Control

RLM control enables users to change the inner/outer eye values to test the DUT's RLM against defined values determined by the testing point and type. These controls are especially useful for determining the output of the modulator/driver/redriver by transmitting a clean signal, checking the level of distortion, and tuning the BERT accordingly, providing calibrated settings for device output.

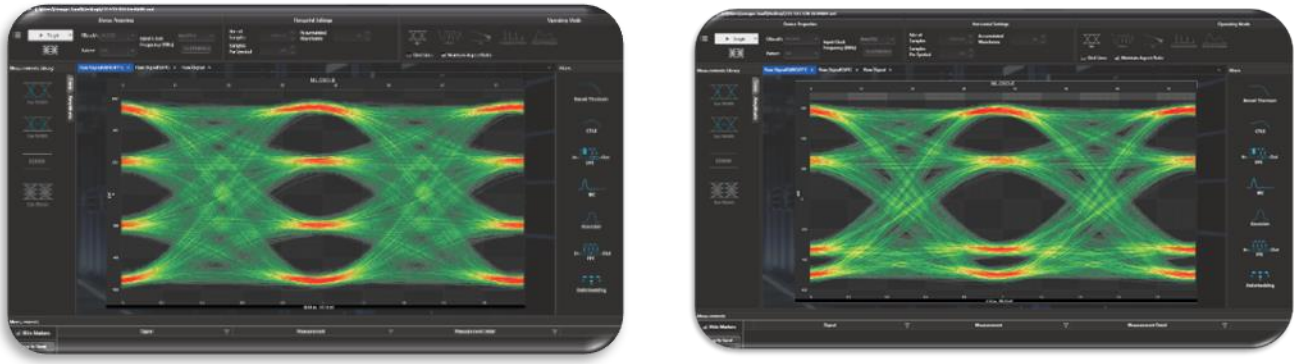


Figure 16: Inner/outer eye control

Shallow Loopback

The shallow loopback function tests the signal generated by the DUT itself by looping through the BERT. The BERT can then equalize the signal for a better BER on the Rx side of the DUT but can also inject noise to determine DUT Rx resilience. The function works with a variety of traffic types including unframed PRBS, framed Ethernet and FEC traffic.

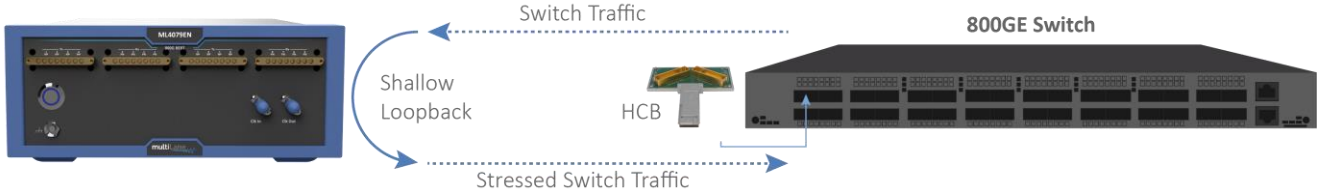


Figure 17: Shallow loopback testing setup

Key Takeaways:

- MultiLane platforms exceed jitter requirements of the IEEE three times over
- Both Automated and Manual JTOL are supported
- ITOL testing is automated with a pass/fail report comparing the BER at selected amplitudes

Setups and Applications

MultiLane responds to the rapidly emerging essential requirements of high-speed interconnect development and validation with a suite of new 800G solutions for a myriad of test and validation use cases.

MultiLane solutions include three fully featured 800G BERTs designed to address a specific industry need:

Figure 18: MultiLane 800G BERT Family

The ML4079EN and ML4054E are specifically designed to add jitter and noise in addition to other capabilities found in their respective datasheets. These instruments support SJ calibration in both FM (frequency modulation) and PM (phase modulation) at 10 different preset frequencies based on IEEE requirements – 40, 100, 400, 1000, 1330, 2500, 7000, 10000 and 12000KHz – also providing the ability to calibrate custom frequencies in-house depending on user need, with injection magnitudes three times higher than the required specifications.

RJ and BUJ are configurable via ThunderBERT. All the different variants of jitter can be injected independently or concurrently. This capability is fully integrated into the BERTs and does not require any external equipment. A thermal stream kit can be mounted onto the ML4054E to facilitate over-temperature testing for pluggable optics and cables.

All these options are enhanced with the MultiLane flagship ThunderBERT GUI, through which the various forms of jitter and noise injection can be established and monitored.

Figure 19: ML4079EN 800G BERT with stress testing features

Host ASIC Stress testing

Hosts must manage multiple sources for potential signal deterioration. Incorporating stress testing into a complete validation cycle, therefore, ensures host resilience in the face of real-world impairments.

Diagnostic Validation and Margin Testing in Shallow Loopback Mode

Figure 20 depicts a ML4079EN accepting traffic from an external 800GE switch, looping the traffic internally and re-transmitting it back to the RX side of the host. This can be used to test the robustness of the host port, by adding an increasing amount of asynchronous crosstalk noise for a clear depiction of where the receiver starts to produce uncorrectable errors.

Unidirectional ASIC Stressed Input Test

In the same setup, an ML4079EN transmits a signal to the HCB and the Switch ASIC. The switch locks on incoming PRBS and reports BER after jitter and noise have been added to the transmitted signal. The shallow loopback feature is widely used for these applications.

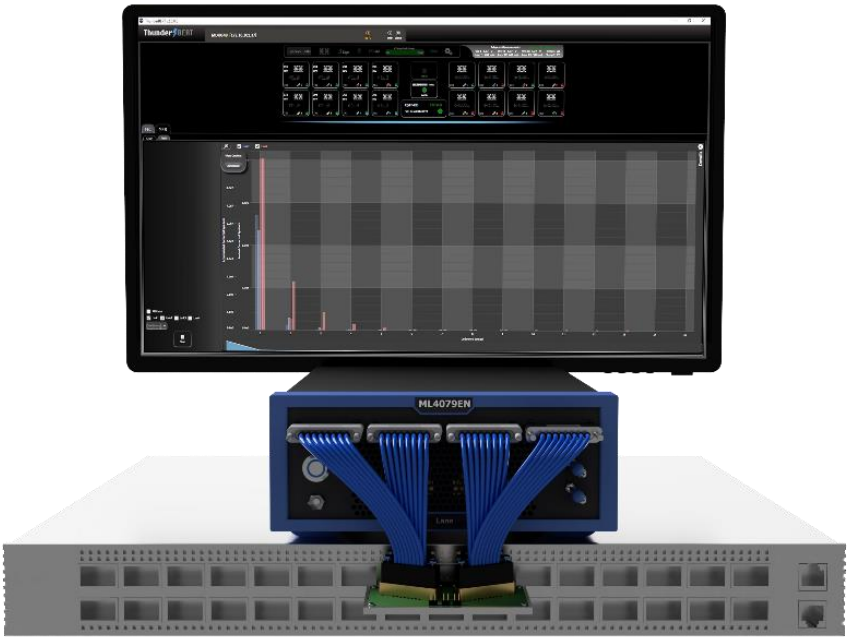


Figure 20: Host testing setup

Transceiver Testing

Transceiver testing needs to cover both spec compliance and field performance, even at the early stages of development. BER testing covers spec compliance but does not account for device performance under less-than-ideal conditions, hence the need to evaluate transceiver performance in the face of jitter and noise. As such, stress testing is performed alongside other electrical and optical Tx and Rx testing to ensure device resilience at every stage.

Electrical Rx Testing

Below is a table summarizing the main receiver electrical tests with jitter and noise injection:

Table 5: IEEE tests requiring jitter and/or noise injection

Publication	Subset of supported Measurements
200G/400G (GAUI-8): 802.3bs Table 120E-3	BER Stress Input Low&High Loss Chanel

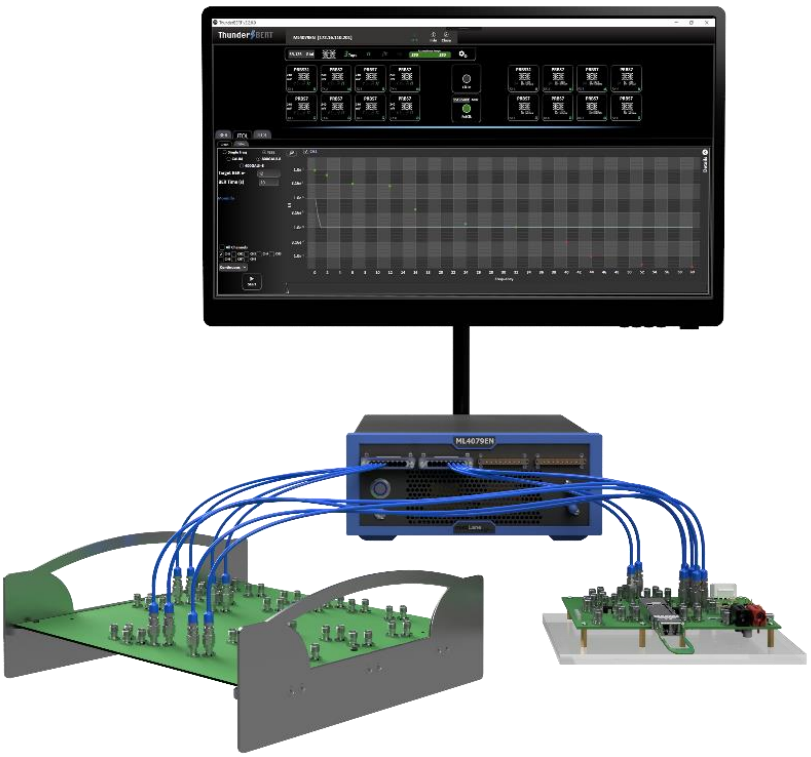


Figure 21: Electrical Rx transceiver testing setup

Module Stressed Input Tolerance: Low/High Channel Loss Conditions

The Stressed input low loss channel is performed using the ML4079EN and ML4062 (QSFP-DD) or ML4064 (OSFP) Module Compliance Board, or the ML4054E and associated QSFP-DD or OSFP adapter. As defined in Table 120G-9 in the IEEE802.3ck and IEEE802.3df publications, sinusoidal, random, and bound uncorrelated jitter are driven into the module under test. The procedure also calls for a frequency-dependent attenuator and counter-propagating crosstalk to be applied. The resulting BER when processed by the PMA (Physical Medium Attachment) must be equal to or better than 1E-15, according to Clause 135 for 100GAUI-1 Chip-to-module signaling, and Clause 120 for 200GAUI-2, 400GAUI-4, or 800GAUI-8 Chip-to-module signaling. The BER is monitored for a set time duration to ensure adequate performance confidence. It is typical, however, for system adopters to define their own higher BER thresholds and longer test durations to pass the IEEE-defined limits with additional margin.

Module stress input tolerance is performed with low loss channels to exercise worst-case reflections, in addition to high-loss channels to exercise the equalization capability of the receiver under test. A high-loss test can be supported with channel emulation via tuning the transmit equalizer of the ML4079EN BERT, or with the ML4067 channel emulation board.

Automatic JTOL can be used for this test since the requested frequencies and the jitter amount are the same for all 200GAUI-4 and 400GAUI-8 tests.

Parameter	Case A	Case B	Case C	Case D	Case E	Units
Jitter frequency	0.04	1.333	4	12	0.40	MHz
Jitter amplitude	5	0.15	0.05	0.05	0.05	UI

Table 6: SJ injection per IEEE

Interoperability Tests

A key part of the 112Gbps/lane testing cycle, system interoperability testing is crucial for transceivers and pluggable testing.

Pre/Post- FEC

This setup assesses the performance of pluggable DUTs in real-life networking environments thanks to diagnostic capabilities of Gigabit ethernet switches. The test procedure, in this case, uses 2 DUTs for multi-vendor comparison. The ML4079EN is equipped with real-hardware KP4 FEC capabilities.

Pre- FEC BER -Testing

DUT1 is in mission mode with the 800G switch used to exchange PRBS traffic with the ML4054E. Both DUTs are connected to a MLO4034 optical attenuator to generate a BER vs. RX Power Curve Report.

Post- FEC Testing

With an identical hardware setup, idle Ethernet FEC traffic (RS (544,514) or RS (528,514)) is exchanged between Switch and BERT instead of a PRBS pattern. The report generated is a FEC SER vs. Rx Power Curve.

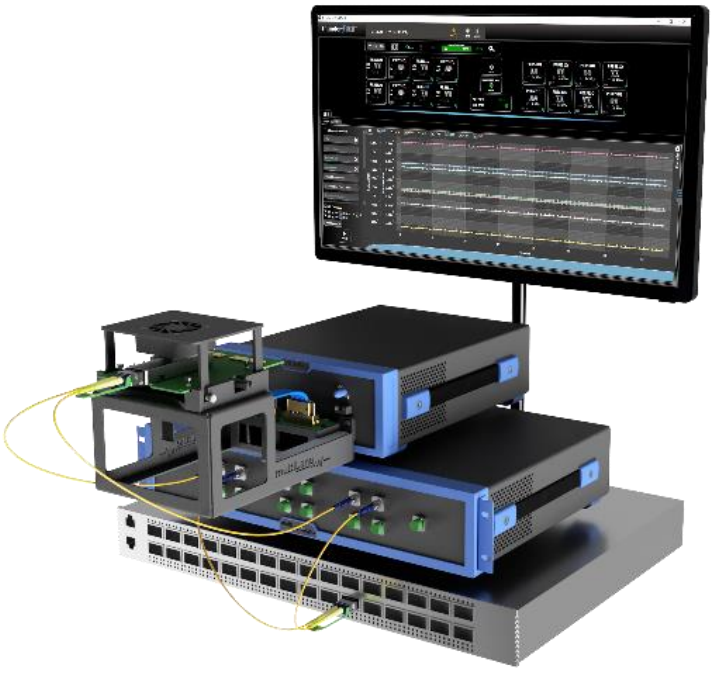


Figure 22: Interoperability test setup

Active Cable Testing: AEC & ACC

ML4054E is an ideal solution for AEC (Active Electrical Cable) and ACC (Active Copper Cable) QSFP-DD and OSFP testing.

BER and SER tests are generated using 2 ML4054E as a signal generator and error detector, jitter and noise can be added to monitor cable behavior. Compliance Test & Validation for the Common Management Interface Specification (CMIS) – which enables interoperability across an increasingly diverse industry – is also supported by the ML4054E.

Figure 23: Active cables test setup

Testing Linear Optical Systems

As the 800G ecosystem matures and the industry begins to develop 1.6Tbps interconnects, more power-efficient data transmission is actively being explored. A strong alternative contender, linear systems use redriver-based signal modulation, as opposed to the established DSP retimer based modules that are currently ubiquitous in Ethernet communication. While dissipating significantly lower power than their retimer-based counterparts, linear systems are exponentially more susceptible to interference and degradation from noise, be it in the form of random noise or crosstalk.

Having a testing setup that can emulate both the potential disruptions of a real-world setup, in addition to the transmit and receiver equalization capabilities of modern host ASICs, is therefore crucial to ensuring the validity of linear systems at 800G and beyond. The MultiLane ML4079EN offers a current turnkey solution to linear system testing. With its suite of noise insertion options, equalization capabilities, and high amplitude swing, the ML4079EN can both drive a signal and verify the effects of noise on the performance of the DUT. The ML4079EN can serve at multiple test points, either as a PPG and/or stress injector at TP1/TP1a, a source of stressed signals at TP3, and a reference receiver at TP2, and TP4a.

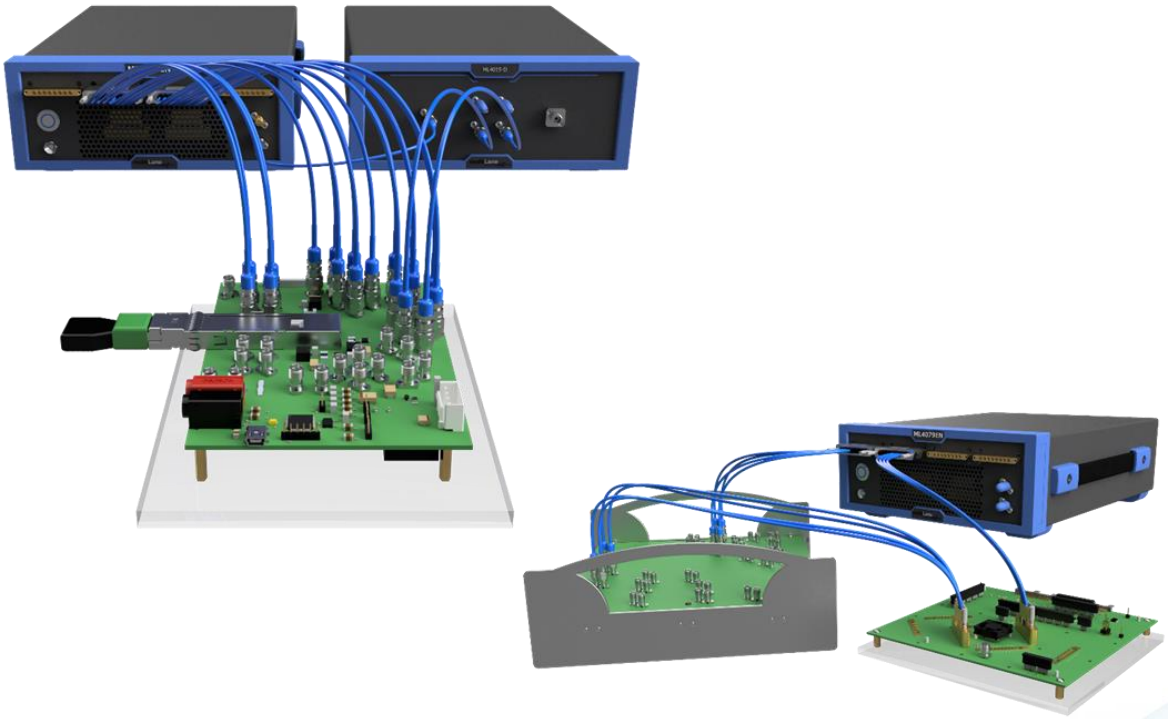


Figure 24: Linear test setups

In Summary

Industry appetite for ever-increasing cloud capacity continues to push the limits of semiconductor and interconnect technologies. The higher baud rates needed to enable port speeds at 800G lead to increased complexities in transmission channels, compelling optical/electrical receivers to adopt advanced equalization routines and hence carry a larger responsibility than ever before. Jitter budgets get tighter and design margins narrower, calling for advanced test and measurement solutions to accelerate design, development, and deployment of 800G ecosystem technologies. Here, advanced jitter and noise testing makes all the difference.

Addressing the need for solutions to account for the various forms of jitter and noise present in high-speed systems, MultiLane has expanded its selection with an array of 800G signal disruption solutions all contained within a single instrument for every stage of industry development – supported by ThunderBERT, which streamlines and provides visual control for test and measurement tasks. MultiLane solutions not only validated DUT robustness in the face of both user-defined and industry-defined signal impairment, but also determine margin of operation compared to the mandated IEEE masks, ensuring manufacturers can be precisely aware of the edge their products provide in a market hungry for robust architecture with minimal failure points.

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