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Innovation for the next generation

ML4054-400 GEN 2

400G BERT Production Tester| QSFP-DD, OSFP, QSFP, SFP-DD, SFP Interfaces | PAM-4 & NRZ BERT|

Benchtop version | Suitable for In-Situ oven tests | Generation 2 |

Summary

The latest introduction to the MultiLane product family is the ML4054-400. It is a fully featured 400G BERT with a native CFP8 port. This instrument is used in testing QSFP-DD and OSFP modules through the CFP8 to QSFP-DD or CFP8 to OSFP adapter. These connector savers are suitable for transceiver testing, since they can be replaced without damaging the native connector. ML4054-400 simplifies production testing by eliminating the external cabling and is designed for 400G applications.

The passive MSA compliant adapters drive the signals between the CFP8 connectors and QSFP-DD/ OSFP connectors. The ML4054-QDD and ML4054-OSFP adapters support all the QSFP-DD/ OSFP features and pin mappings. At the receiver side, an octal port CDR device is implemented, able to recover up to 53.125 Gbps PAM4 signal or 26.5625 Gbps NRZ signal.

MultiLane offers a number of other adapters as well, such as for instance: CFP8 to QSFP, CFP2DCO, SFPDD and SFP. The exposed adapter can function in a wide range of different temperatures.

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ML4054-400 GEN 2

400G BERT Production Tester

Introduction

The ML4054-400 is a fully featured 400G BERT. It has a native CFP8 port and uses CFP8 to QSFP-DD, OSFP and other adapters that are at the same time connector savers and are suitable for testing in an oven and can be replaced by the customer on the fly.

This instrument facilitates production testing since no external cabling is needed. It comes in two different form factors: benchtop and low profile. The low-profile version can be directly mounted on the door of the temperature chamber (cf. description below).

The GUI allows you to individually control each TX level, equalization, eye balance, pattern and coding. The user may also inject error sequences into the stream. The receiver features CTLE and FFE equalization for up to 14 dB of loss at Nyquist; it also allows advanced troubleshooting capabilities.

Key Features

▪ Low cost, instrument-grade BERT optimized for high speed data analysis of 200G/400G transceivers.
▪ Native CFP8 interface.
▪ Adapters available CFP8 to QSFP-DD, OSFP, and a host of other types
▪ Integrated BERT and CFP8 host controller enables:
  o RX CTLE tuning
  o TX Equalization control
  o Current sensing per module
  o Voltage sense
▪ Ability to tune the bit rate in very fine steps to facilitate finding the locking margin.
▪ Excellent insertion loss characteristics of the connector saver (cf eye diagrams below)

▪ Supports PRBS13Q/31Q and user-defined patterns.
▪ Performs all the measurement functions of the BERT, and a QDD/OSFP/others host in terms of I2C control for configuration, monitoring and functions.
▪ Features industrial components, suitable for reliability testing inside an oven over a wide temperature range.
▪ Low power consumption.
▪ API library, sample code and Python wrapper.

Target Applications

▪ Production testing of transceivers
▪ Benchtop testing for functional and SI functionality
▪ On-the-go testing of transceivers in the field
▪ The exposed adapter can be used from -5 to 85C for in-situ AC tests
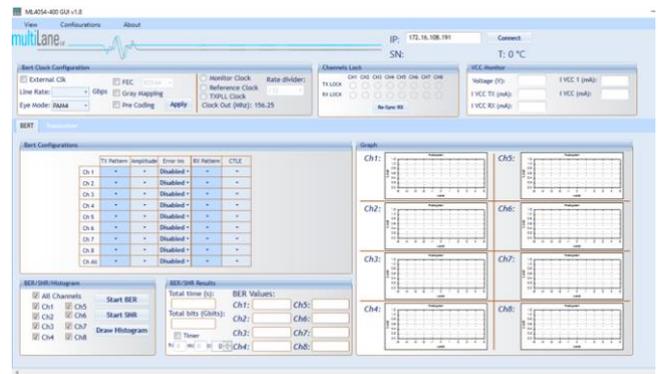▪ Transceiver functional tester, for simple validation

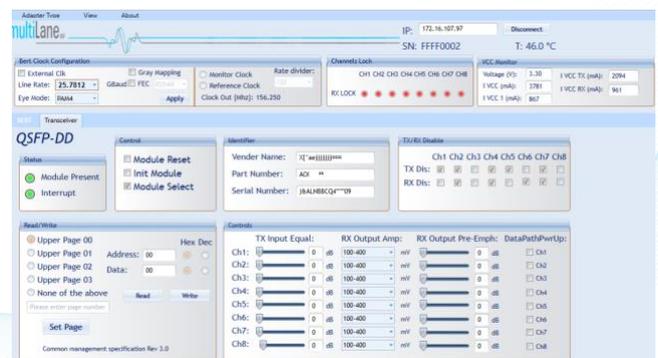

Figure 1: ML4054 GUI – BERT tab

Figure 2: QDD MSA Control Menu
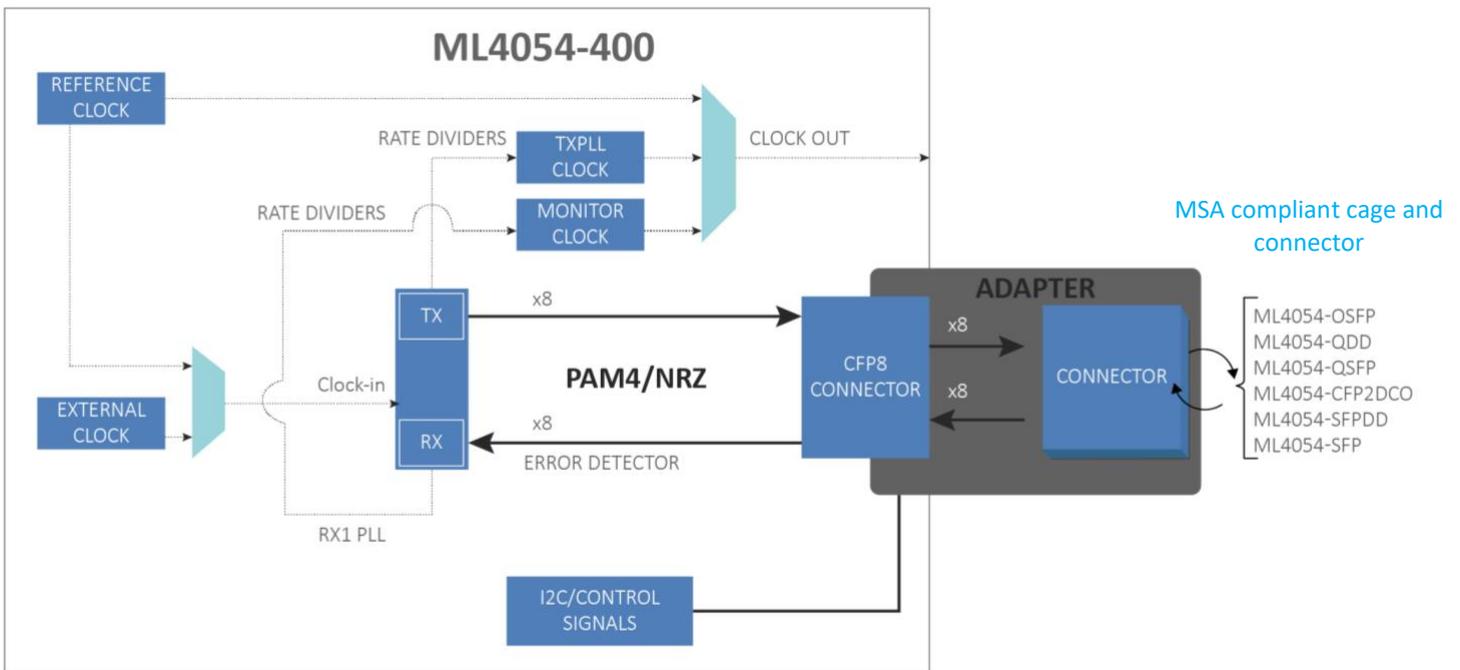
Block Diagram – Schematic

Figure 3: ML4054-400 with adapters

ML BERT GUI

This GUI is intuitive, featuring multiple and single layouts of bathtub and eye contour.
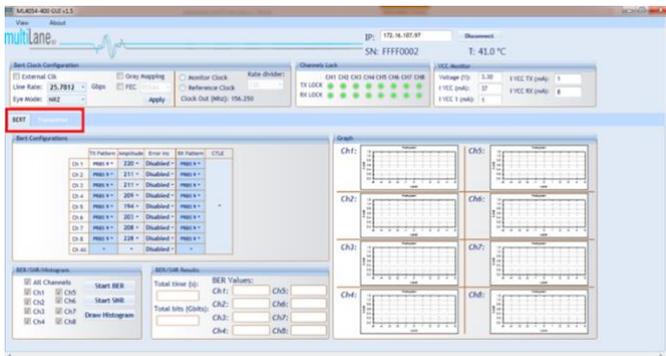

Figure 4: Main GUI

Low-profile Version

Features the same hardware inside a special enclosure that mounts on the door of a MultiLane-approved temperature chamber, which is part of MultiLane's MLT8000 thermal solutions.

Figure 6: Low profile ML4054-400, mounted on custom oven door (MLT8000)
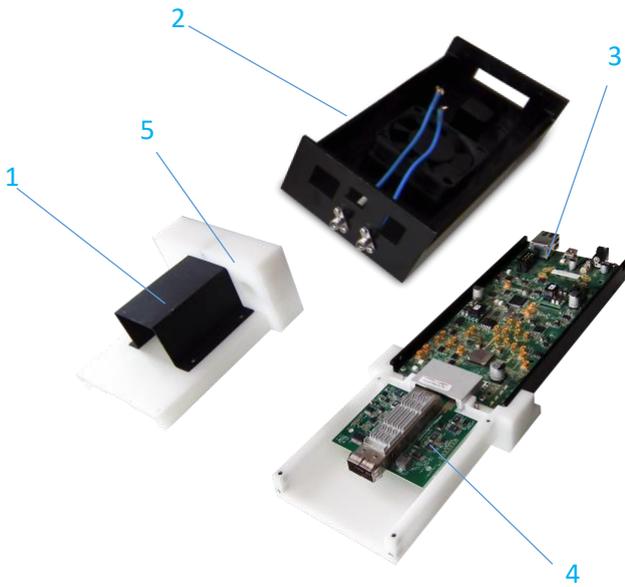

Figure 5: Low profile ML4054-400

Figure 7: Exploded view of the ML4054-400-LP

1. Fan cover, fan suction air duct
2. ML4054-400 cover, Metal
3. Ethernet to instruments
4. Connector saver to 400G host module adapter + transceiver
5. Cassette FR4, upper part

Available Adapters

- ML4054-OSFP
- ML4054-QDD
- ML4054-QSFP
- ML4054-CFP2DCO
- ML4054-SFPDD
- ML4054-SFP

Figure 9: ML4054-QDD

Figure 8: ML4054-OSFP
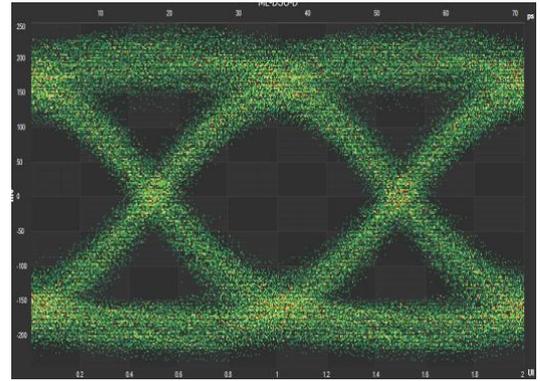

Figure 10: ML4054-QSFP

Figure 11: Raw un-equalized 28 Gbps Signal after passing through the QDD adapter followed by a QDD HCB and 40 cm SMA cables

Figure 12: ML4054-400-BTP front

Figure 13: ML4054-400-BTP back

Electrical Specifications

Details	
Bit Rates	PAM-4: 22 – 28.125 GBaud NRZ: 1.25 – 3.125 & 5.15 – 28.125 Gbps
TX Amplitude Differential	0-800 mVpp
Patterns	PRBS 7/9/11/13/15/16/23/31 /58 PRBS13Q/31Q and SSPRQ Square wave
TX Amplitude Adjustment	Steps of 2 mV
Pre-Emphasis Resolution	±1000 steps
Equalizing Filter Spacing	1UI
Random Jitter RMS	TBD
Rise / Fall Time (20–80%)	15 / 15 ps
Coding	DFE Pre-coding Gray coding FEC –KP4, -KR4
Error Detector sensitivity	TBD
Error Detector CDR	Supported
Error Detector Equalizer	10 tap with gain and offset compensation. 3pre- and 6 post-cursors Or 1 tap FFE slicer And 1 tap optional DFE filter And Optional 16 tap reflection canceller And Level-dependent equalizer for the inner eye levels
Input Equalizer Dynamic Range	Up to 30 dB
TX/RX connectors	QDD or OSFP or upon request
Reference clock Output	TBD
Eye histogram resolution	8 bits horizontal across 2UI / 9 bits vertical
Clock Input Range	Rate dependent
Clock Input Amplitude	200 - 1200 mV
Clock Input Impedance	50 Ω
Temperature range	-15 to 75 °C
Weight	~1.5 kg
Dimensions LxWxH (cm)	40 x 22 x 9
Adapter mating cycles	Over 300 cycles

Ordering Information

Details	Product Number
Benchtop version	ML4054-400-BTP
Low profile version	ML4054-400-LP
Thermal chamber kit	ML4054-400-TK
CFP8 to QSFP-DD adapter	ML4054-QDD
CFP8 to OSFP adapter	ML4054-OSFP
CFP8 to QSFP adapter	ML4054-QSFP
CFP8 to CFP2DCO adapter	ML4054-CFP2DCO
CFP8 to SFPDD adapter	ML4054-SFPDD
CFP8 to SFP adapter	ML4054-SFP