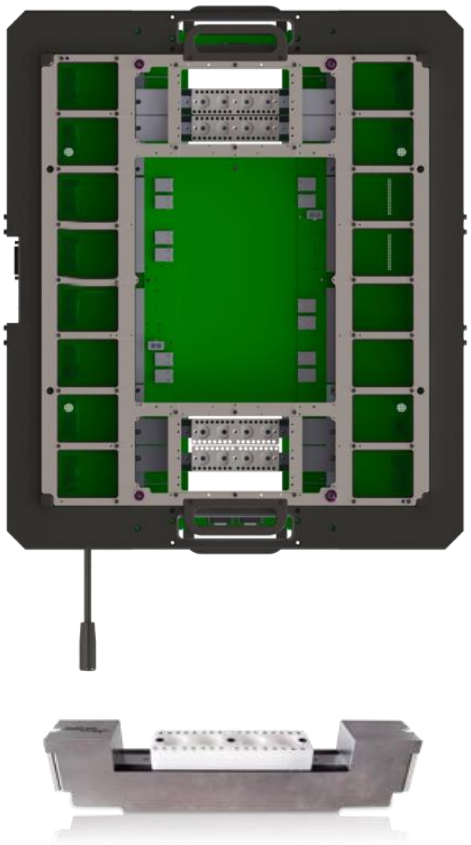
USER MANUAL

multiLane

AT93000 System User Manual

System Overview



Innovation for the next generation

Notices

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers.

Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate with Suspected Failures.

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry

⚠ *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Contents

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Overview of the Advantest V93000 High Speed I/O (HSIO) Test System

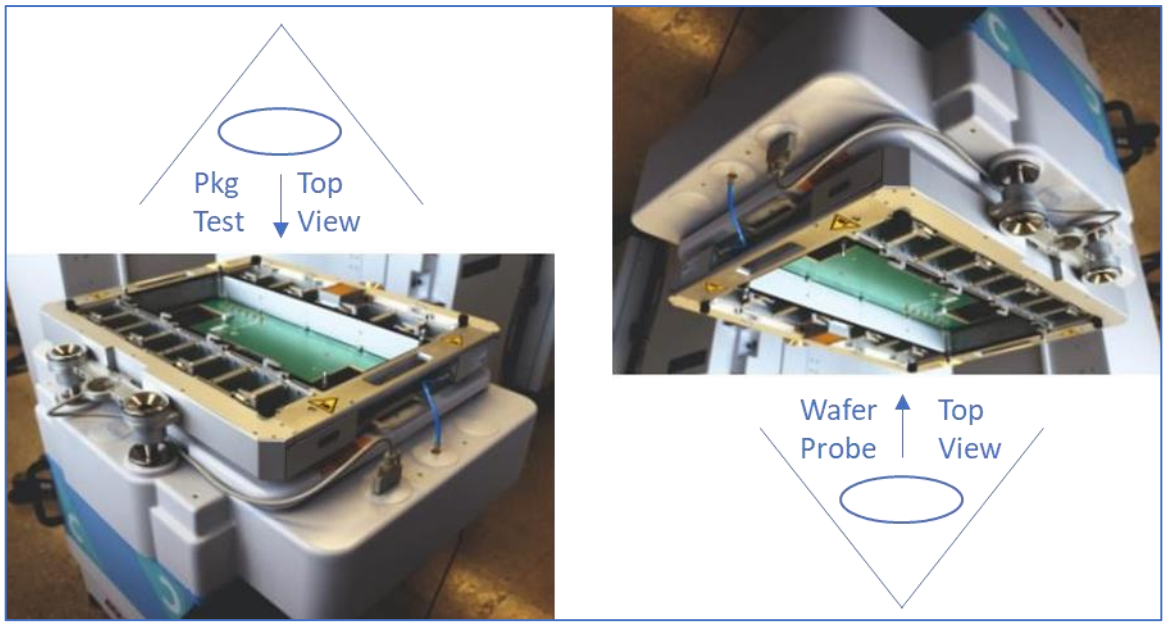


Figure 1: V93000 CTH testhead with Multilane TFRAME attached on top

The Advantest V93000 High Speed I/O (HSIO) Test System allows V93000 users to source and measure DUT signals up to 56GBaud PAM4. See the AT93000 brochure for information about this HSIO test system feature located at [V93000 ATE Test Solutions | MultiLane (multilaneinc.com)]

In Figure 1, the AT93000 twinning frame (TRAME) is hard docked on top of a V93000 test head. The AT93000 is compatible with CTH and STH Advantest V93000 testheads. The user's DUT loadboard is hard docked on top of the TFRAME and the device handler or wafer prober is hard docked to the DUT loadboard. For wafer probe, the TFRAME would be upside down from this picture. Figure 1 shows the HSIO[1] twinning frame docked to a CTH testhead with one of sixteen populated Pogo Segments. An exploded view of these individual pieces is shown in Figure 2, including up to four Multilane instrument cassettes.

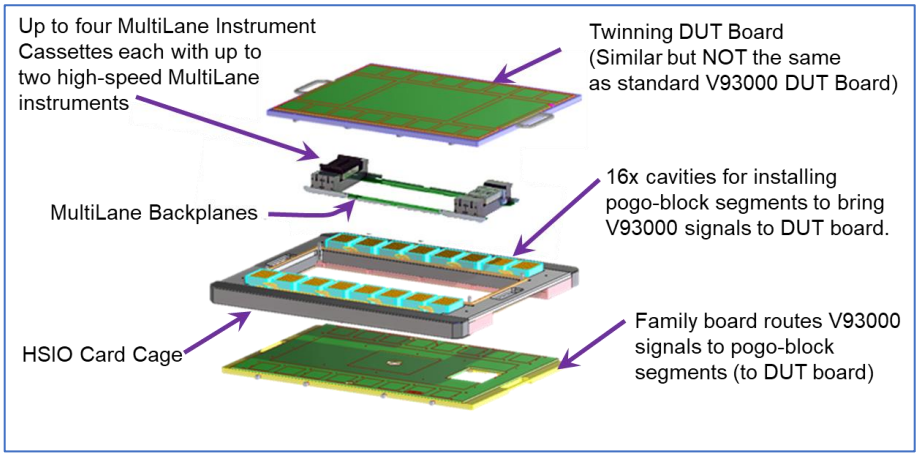


Figure 2: Building blocks of the Multilane TFRAME

[1] HSIO is an ATE industry acronym for "High Speed Input/Output". The AT93000 is an HSIO solution

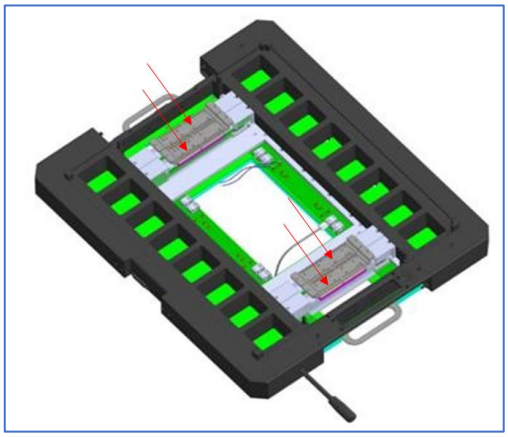


Figure 3: TFRAME with red arrows pointing to the 4 Multilane cassettes

The main advantage of the ATE system as compared to using benchtop instruments, is that the signal path between DUT and Cassette instruments is considerably shorter thus minimizing insertion and return losses. The AT93000 channel density maximum is up to 32 channels if all 4 cassettes are fully populated.

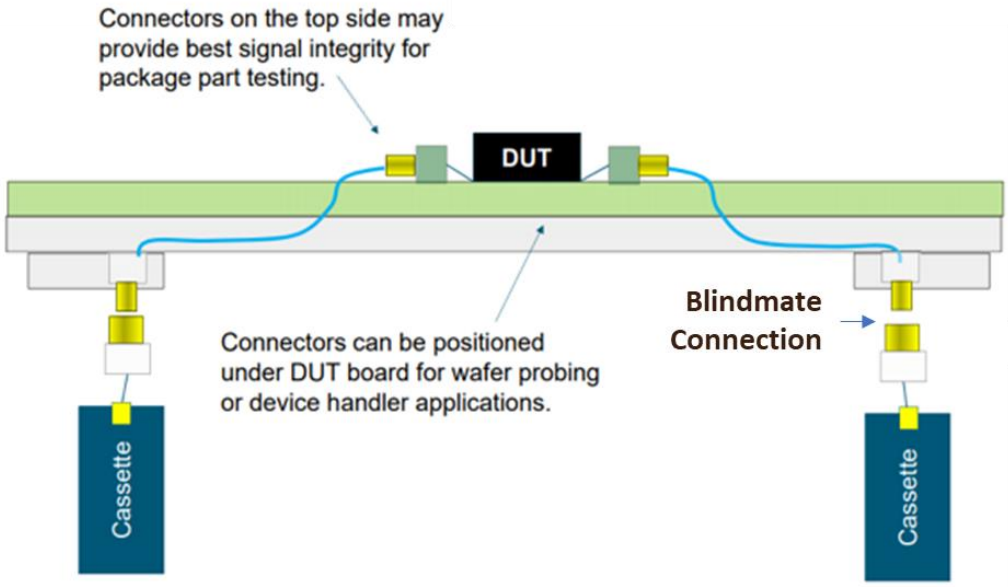


Figure 4: AT93000 signal paths from instruments to DUT

Each of the four Multilane cassettes contains either one or two Multilane high-speed instruments. Refer to each instrument's User Manual for the blindmate connector pinout of that instrument in the cassette. Instrument manuals and datasheets can be found at ATE | MultiLane (multilaneinc.com). Figure 5 shows one side of a cassette with the protective cover removed. This exposed PCB is a 4-channel (differential) Multilane instrument. The other side of the cassette can have a second 4-channel Multilane instrument for a total of 8 differential channels per cassette. Figure 5 also shows the backplane connector. User Manual pinouts are referenced to this connector. The instrument on the opposite side of the cassette is facing into the page so that its backplane connector is located on the backside, lower left corner. For example, a cassette might contain a 4-channel AT4039D BERT on side 1 of the cassette and a 4-channel AT4025 DSO on side 2 of the cassette. In the case of 8-channel instruments, like the 8-channel AT4079B BERT, there will only be one 8-ch instrument in the cassette with one connector due to blindmate 32-pins limitation.

Figure 5: Instrument Cassette with protective cover removed

Figure 6 shows the AT93000 area located under the docked device loadboard.

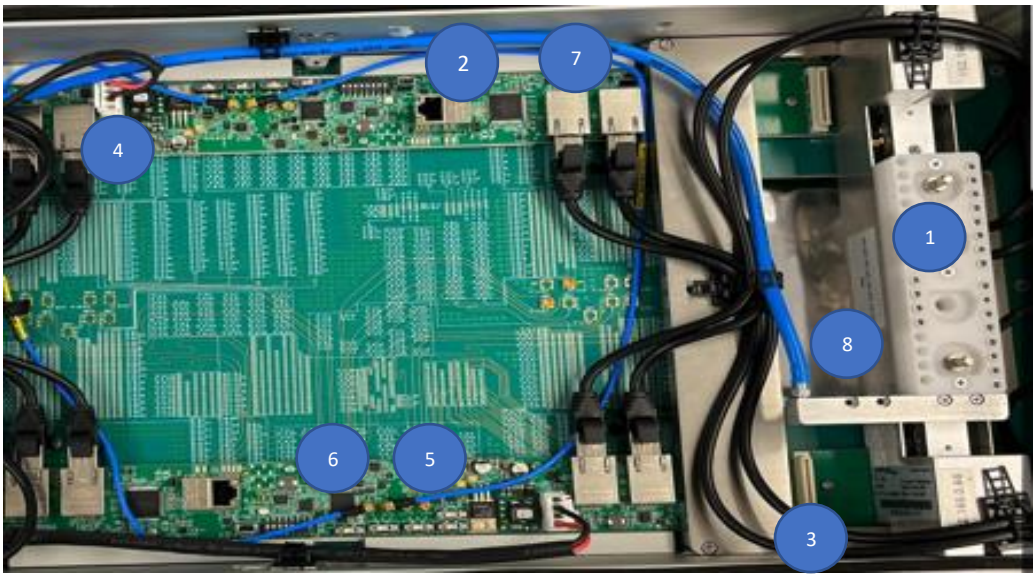


Figure 6: AT93000 Cassette Area

	Item	Description of Items in Figure 6
1	**Cassette**	See: Figure 5: Instrument Cassette with protective cover removed, page 7 See: Cassette and Backplane Location References, page 8
2	**Backplane**	Two backplanes – one at top and one at bottom Provides power, communication, and clock sync to the cassettes See "Cassette and Backplane Location References", page 8
3	**Backplane connectors**	Instrument PCB's inside cassettes plug into these connectors
4	**Power connector**	12V, 6.5A each backplane for a total requirement of 13A external power supply
5	**Clock out**	Clock cabling between backplanes See "Master/Slave Clock Sync Configuration on AT93000 backplanes", page 9
6	**Clock In**	Clock cabling between backplanes See "Master/Slave Clock Sync Configuration on AT93000 backplanes", page 9
7	**Ethernet**	See "Ethernet Connections and IP Addressing" on page 15
8	**Air Intake**	(not shown in picture). Air intake used to cool the cassettes. See "Air, Power, and Ethernet sources" on page 14

Table 1 : AT93000 Pieces

Cassette and Backplane Location References

For consistency across all customer configurations, the backplane and cassette reference numbers are arbitrarily chosen to be defined as shown in Figure 7. The sixteen quadrants labeled 1A to 8B are Advantest defined labels[2]. The "arrow up" engravings on the twinning frame are referenced as pointing "UP". Instruments on the right side of cassettes are plugged into backplane 2. Instruments on the left side of cassettes are plugged into backplane 1. User documentation should be provided to explain to the cassette installer which direction to plug in the cassette. The backplane that an instrument is plugged into also effects the Master Clock synchronization scheme. See "Master/Slave Clock Sync Configuration on AT93000 backplanes" on page 9.

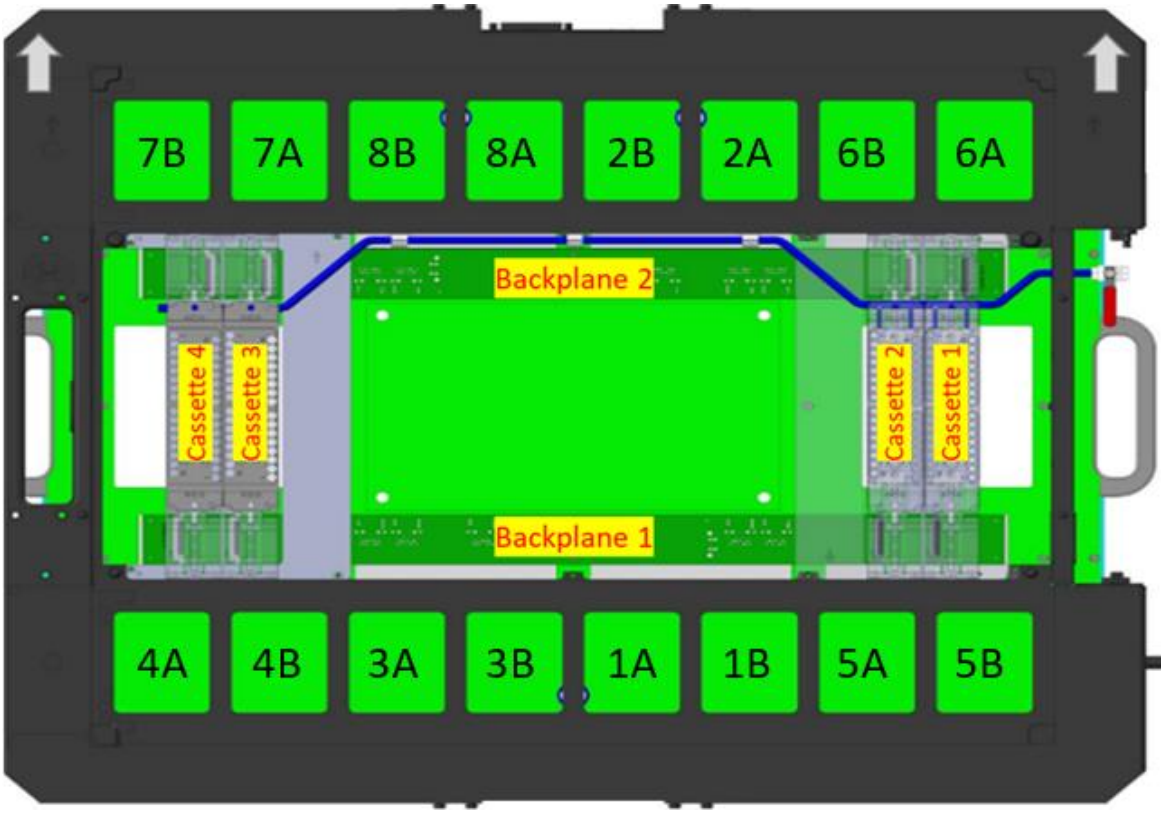


Figure 7: (Top View) AT93000 Backplane and Cassette numbering

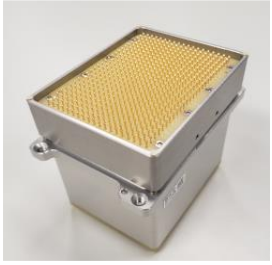


Figure 8: Pogo Block, ordered through Advantest. Part number E8028-PSD

[2] A subset of these quadrants brings the V93000 resources up to the loadboard. Advantest P/N E8028-PSD

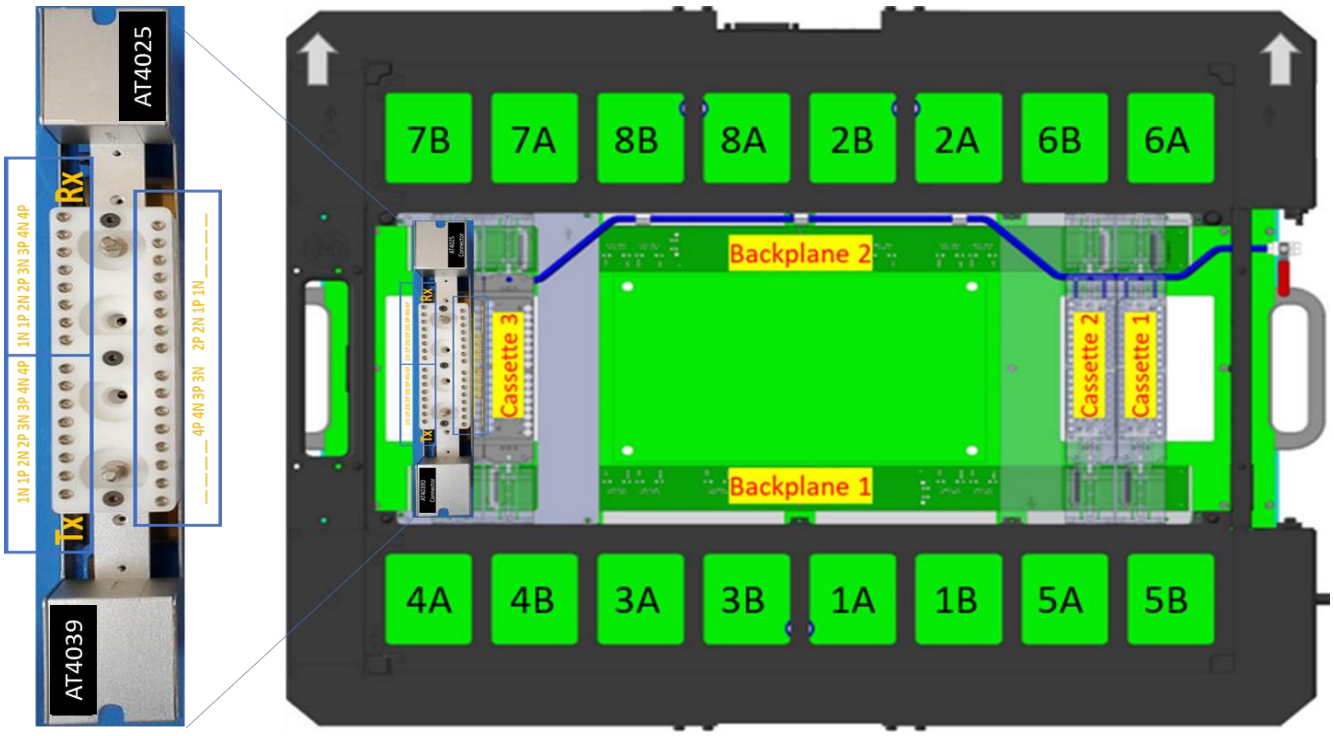


Figure 9: Cassette 4 populated. AT4039 plugs into Backplane 1. AT4025 into Backplane 2.

Master/Slave Clock Sync Configuration on AT93000 backplanes

A master clock can either be generated by one of the installed BERT instruments or by a clock from the DUT loadboard. There can only be one clock master for synchronizing all BERTs and DSOs on each backplane. All other instruments on that backplane operate as clock slaves and will synchronize their operation to the instrument or loadboard master clock. The Master/Slave clock configuration is controlled through switch settings on backplane 1 and backplane 2 and is explained later in this section.

If the clock is coming from the DUT or V93000, then all cassette instruments will be slaved to the external master clock. In this case, the external differential clock[3] should be cabled to the "clock-in" SMP connectors on the backplane having the slaved instruments, using two high-speed cables. Check Multilane instrument datasheets for maximum clock sync frequency. For explanation how to send DUT clock signals to the ML backplanes via family board, see Multilane Family Board Documentation.

Backplane Switch Settings

Backplane switches control which instrument clock (or loadboard clock) controls the clock synchronization between instruments[4]. There are switches and switch straps on each backplane.

[3] Single-ended clocks coming from the DUT loadboard are not supported. They must be differential.

[4] For older backplanes, refer to

The switch straps are for *Multilane internal use only* and should never be changed from what is shown in Figure 10.

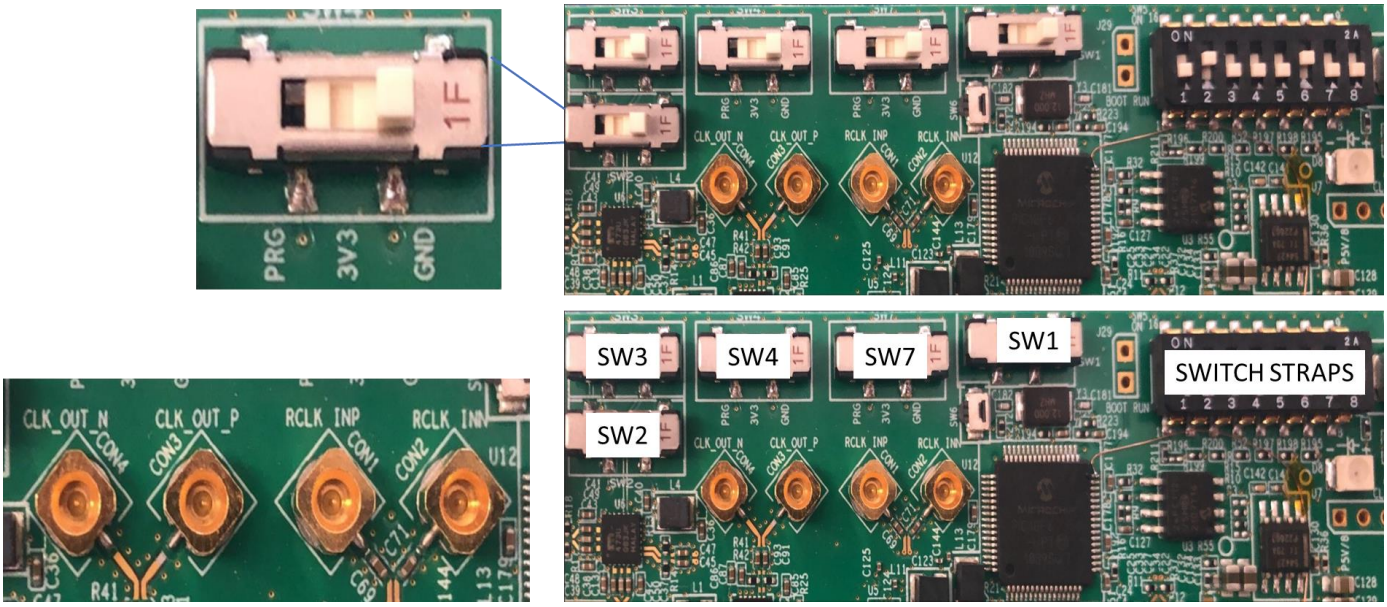


Figure 10:SPMP Clock Connectors on ML Backplanes 1 and 2

The ML backplane SMPM connectors are shown in lower left picture of Figure 10. Cables can either connect from backplane 1 to backplane 2 or to the family board as shown in Figure 11. The family board connections go up through the G1A Advantest pogo block and are available to be connected on the DUT loadboard.

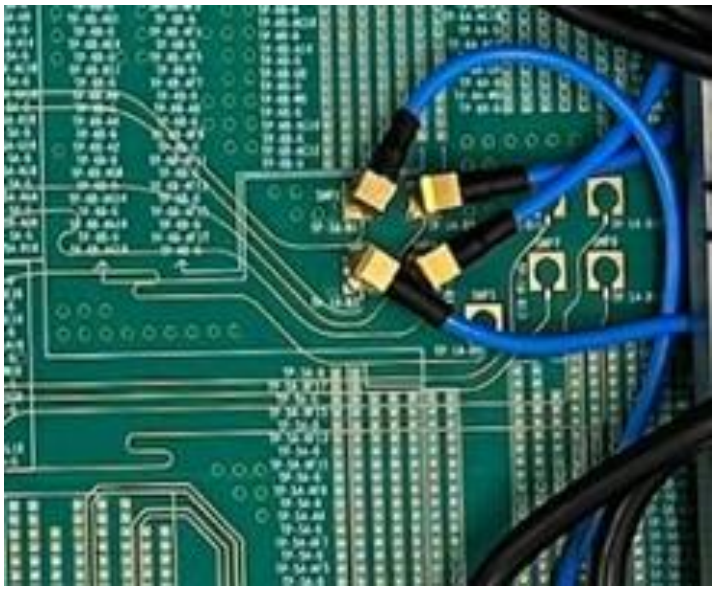


Figure 11:SMPM Clock Connectors on Family Board

Referring to Figure 10, each of the 5 switches on each backplane control the master/slave modes by one of two methods:

Appendix: Older Revision Backplane Clock Jumper Settings on page 17.

1. **Manually**: Set each switch to either 3V3 or GND
2. **USB Programming Mode**: Set all switches to PRG

Setting Master/Slave Manually

Set the 5 switches on each backplane using Figure 1Figure 12 and the table in Figure 13.

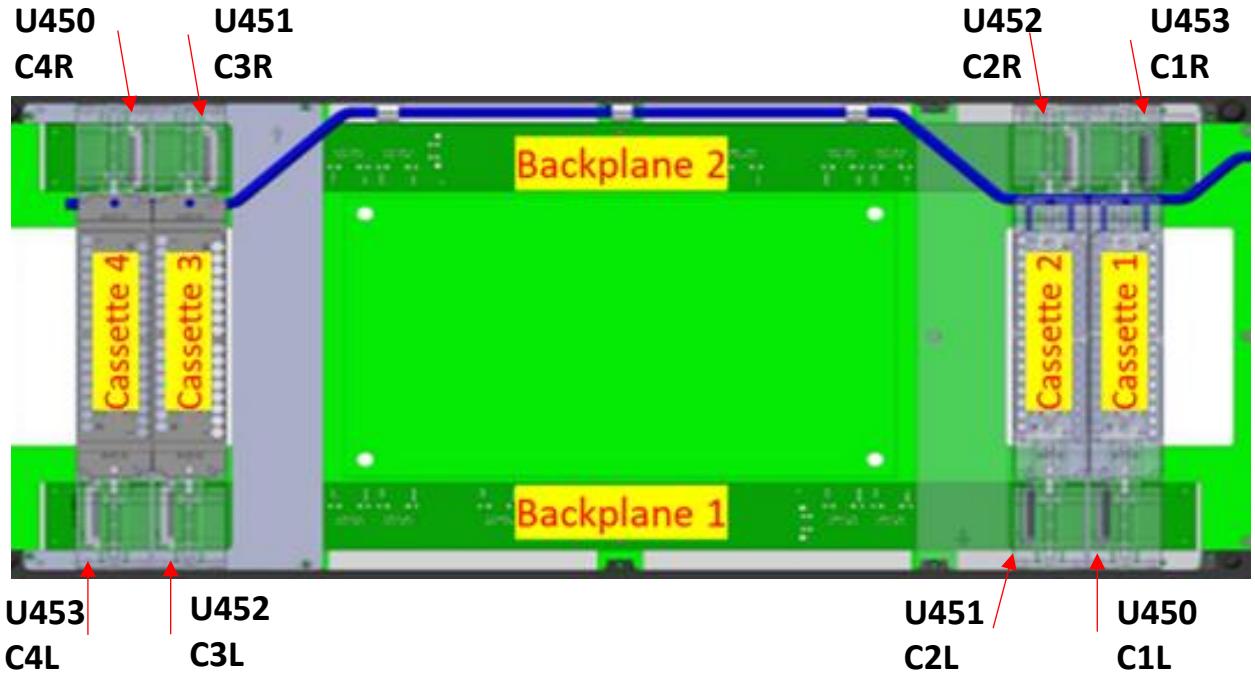


Figure 12: Backplane Reference Designators.

	U450 is MASTER	U451 is MASTER	U452 is MASTER	U453 is MASTER	All U45x SLAVE
Backplane 1	C1L	C2L	C3L	C4L	All Slave
Backplane 2	C4R	C3R	C2R	C1R	All Slave
SW1	0	0	0	1	0
SW2	0	0	1	0	0
SW3	1	0	0	0	0
SW4	0	1	0	0	0
SW7	1	1	1	1	0

Figure 13: Manual Mode Master Slave Switch Settings

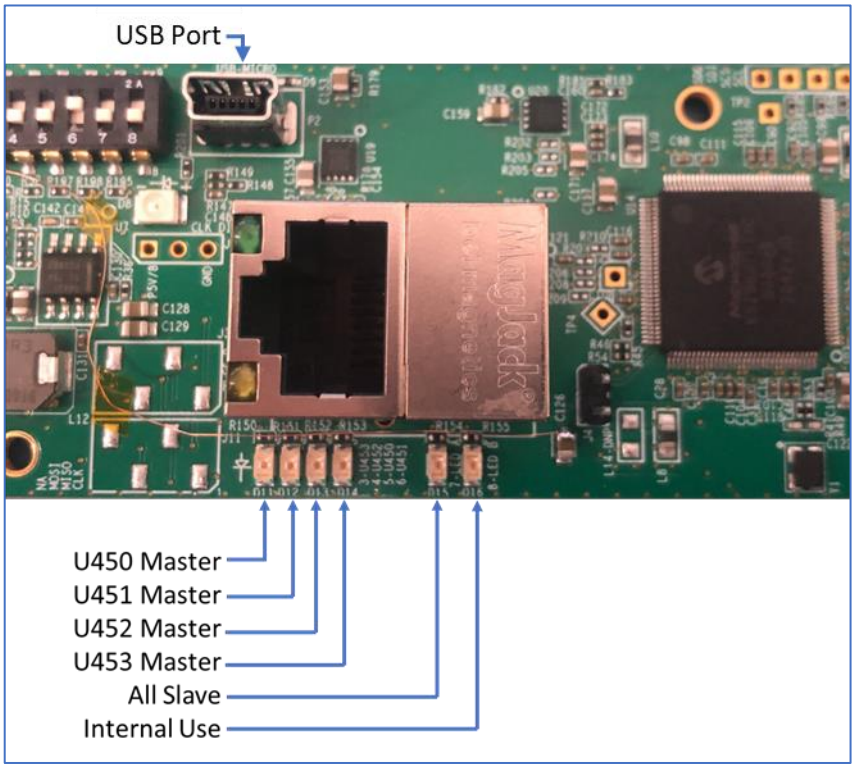


Figure 14: Backplane USB and Master/Slave LED light indicators

Setting Master/Slave using USB Programming Mode

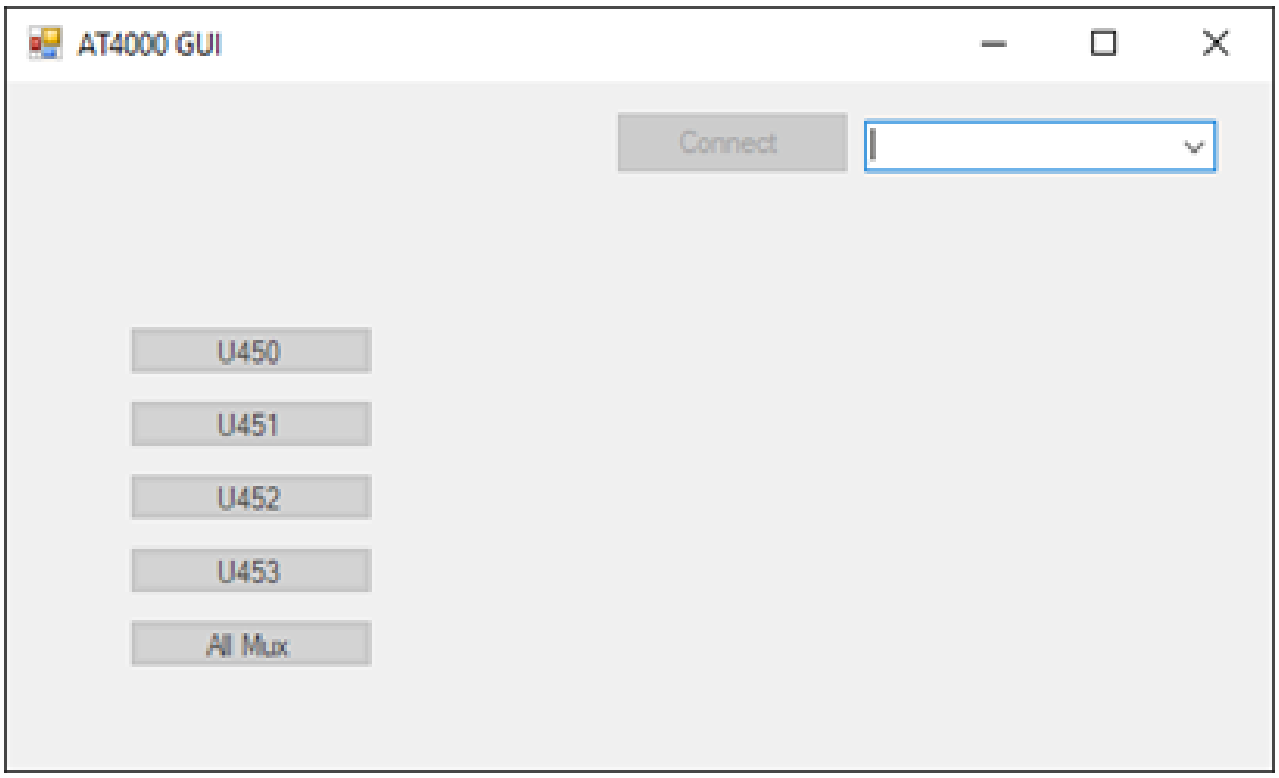
Contact Multilane if USB Programming Mode is to be used.

Step 1: Set all switches to PRG

Step 2: Connect laptop to USB port shown in Figure 14

Step 3: Obtain ML AT4000 GUI

Step 4: Use GUI shown in Figure 15 to set one of the instruments as the master or to set all the instruments to slave. When all slave, the expectation is that the master will either be coming from the other backplane or from the DUT loadboard via the family board



	U450 is MASTER	U451 is MASTER	U452 is MASTER	U453 is MASTER	All MUX
Backplane 1	C1L	C2L	C3L	C4L	All Slave
Backplane 2	C4R	C3R	C2R	C1R	All Slave

Figure 15:GUI for Master/slave config.

Family Board

The Multilane family board, AT93000-1900002, is a general-purpose solution and is optimized for high-speed devices with lower digital pin counts and lower current requirements. If this Family board does not suit your application and you require a different selection of V93000 tester resources, a custom family board will have to be designed.

V93000 mapped resources through the AT93000-1900002 are as follows:

- 11x PS1600 (1408 pins)
- 3x PS9G (192 pins)
- 4x DPS64 (256 supplies)
- 2x DPS128 (256 supplies)
- 2x UHC4 (8 supplies @ 40A)
- 1x MBAV8

Contact Advantest for further information about V93000 tester resources. More information about the AT93000-1900002 Family Board can be found at [AT93000-1900002 | MultiLane (multilaneinc.com)]

Air, Power, and Ethernet sources

The AT93000 cassette instruments are

- Cooled using compressed air
- Powered from an external +12V supply
- Communicated with through ethernet

All these system resources are supply by an external utility box. Refer to the Utility box manual at AT93000-UBOX | MultiLane (multilaneinc.com)

Site Preparation and Installation

Refer to the site preparation and installation manuals at V93000 ATE Test Solutions | MultiLane (multilaneinc.com)

Docking the TFRAME to the V93000 testhead

The AT93000 weighs approximately 35Kg, so some type of mechanical lift assist may be required. For additional information on using a mechanical lift to assist with docking the TFRAME, refer to Advantest Service Documentation, Topic 342435, “Lifting the Twinning equipment”.

Figure 16:AT93000 twinning lift described in the Advantest documentation

Ethernet Connections and IP Addressing

Multilane instruments are controlled by individual IP addresses. IP addresses are hardcoded and are not dynamically assigned at runtime (DHCP). For help choosing the appropriate ethernet connections for each instrument, contact Multilane at ATE-FAE@multilaneinc.com

Software installation when controlling AT93000 via V93000 Smartest

Refer to the site preparation manual at V93000 ATE Test Solutions | MultiLane (multilaneinc.com)

Customer Loadboard

Refer to Final Test or Wafer Test loadboard documentation at Final Test Loadboard and Wafer Test Loadboard

Appendix: Example Customer Documentation

Here is documentation that Multilane uses to guarantee consistent customer configurations leaving our factory. Items in RED are unique for each assembly. The items in RED here are an example and should be changed to match the customer's assembly requirements

Multilane Twinning Frame Assembly Form

Twinning Frame Serial #:	
Customer Contact Name, Email, Phone #:	
Final Inspection By:	Date: Click or tap to enter a date.
Shipping To:	
NOTES:	

	AT40xx Part Num	IP address	Firmware Rev	FPGA Rev	Serial Number	Original IP address
C1R	AT4080	192.168.0.69				
C1L	EMPTY					
C2R	AT4039E	192.168.0.68				
C2L	EMPTY					
C3R	EMPTY					
C3L	EMPTY					
C4R	AT4025	192.168.0.65				
C4L	AT4025	192.168.0.64				
PDU		192.168.0.51				

	B1	B2
Bypass Mode	Yes	Yes

Jumpers (0 or 1)	Mode	SW1	SW2	SW3	SW4	SW7
B1	All Slave	0	0	0	0	0
B2	All Slave	0	0	0	0	0

Coax Cable FROM / TO	B1-CON1 CLKIN+	B1-CON2 CLKIN-	B1-CON3 CLKOUT+	B1-CON4 CLKOUT-	SMP1 B1	SMP2 B3	SMP3 B5	SMP4 B7
B2-CON1 CLKIN+							X	
B2-CON2 CLKIN-								X
B2-CON3 CLKOUT+								
B2-CON4 CLKOUT-								
SMP1 TP-1A-B1	X							
SMP2 TP-1A-B3		X						
SMP3 TP-1A-B5								
SMP4 TP-1A-B7								

Appendix: Software installation when controlling AT93000 via PC

The AT93000 can also be controlled via a PC by connecting the Ethernet ports to the PC
PC minimum hardware requirements are as follows:

- Windows XP SP3 or greater
- Minimum 2 GB RAM
- 1 Ethernet card to establish connection with the device (2 Multilane ethernet ports)
- Pentium 4 processor 2.0 GHz or greater
- .NET Framework 4.0

PC software installation follows. To use an ML instrument under Windows XP, Windows 7 and Vista, it is important that the correct start-up sequence is followed:

- Ensure Microsoft .NET Framework 4.0 is installed
- Install the instrument GUI software from MultiLane's public website
    - Go to ATE | MultiLane (multilaneinc.com)
    - Scroll down: MultiLane Instruments for V93000 → Click on any instrument (eg, AT4039E)
    - You will find the instrument GUI here

- Connect the power cable to the faceplate
- Change the IP of the instrument to fit in the network range
    - Multilane instruments come with preassigned IP addresses
    - The IP address can be manually changed via their GUI
    - DHCP is not supported
- Communication through Ethernet port is required for data acquisition
- Connect the ethernet cable to the faceplate. Depending on instrument installation, 2 ethernet connections may be required
- Now the instrument is powered up, having the right IP, the Ethernet cable links the instrument to the PC with the GUI correctly installed
- To open the GUI, double click on the software icon located in the Desktop directory

Appendix: Older Revision Backplane Clock Jumper Settings (AT4000 REV B)

The AT4000 REV B backplane uses jumpers instead of switches to control MASTER/SLAVE clock selection.

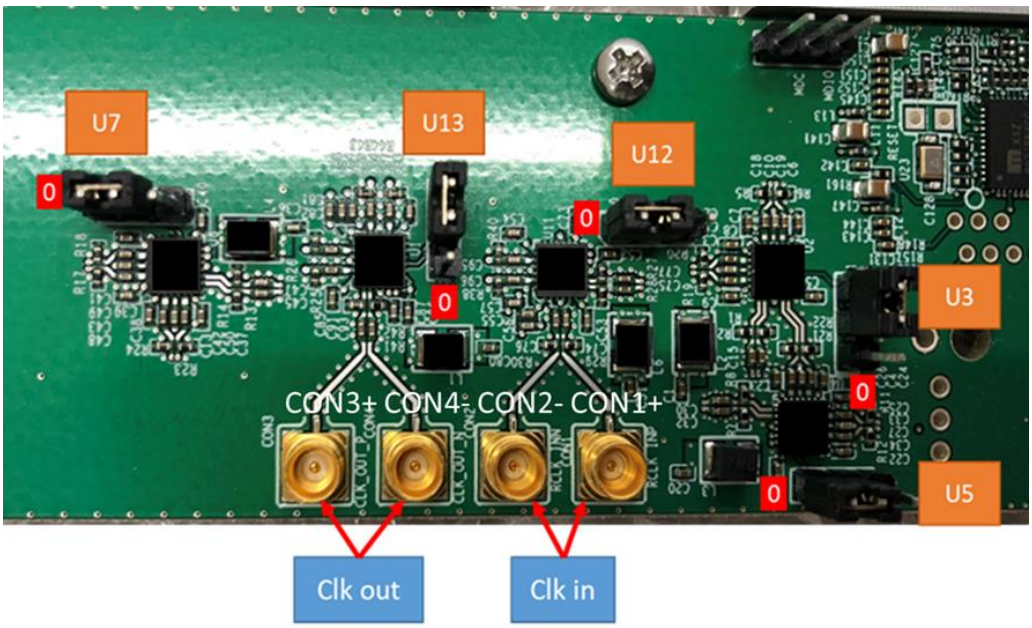


Figure 17:AT4000 REV B Backplane

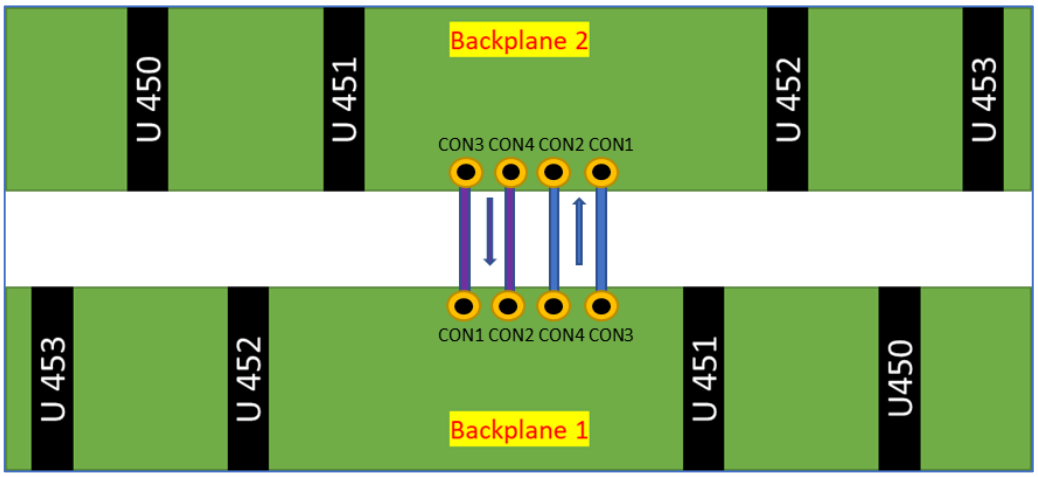


Figure 18:AT4000 REV B cable connection options between backplanes

To set MASTER/SLAVE, refer to the following table:

	U450 is MASTER	U451 is MASTER	U452 is MASTER	U453 is MASTER	All U45x SLAVE
U3	0	0	1	1	0
U5	1	1	0	1	1
U7	1	1	0	0	0
U12	1	1	1	1	0
U13	0	1	0	0	0

Rev. No.	Amendments		Revision date
	Section	Description	
0.9		Initial revision uploaded to Multilane website	
0.9.1		Added appendix “Loadboard reference designators” Added cassette #’s	Jan 14 2021
0.9.2		Changed U13 to “0” for “ALL SLAVE” configuration	March 2, 2021
0.9.3	Appendix 4	Added Appendix showing system block diagram	Oct 26, 2021
0.9.4	All	Updated all sections to reflect ECO changes made in 2022	Oct 11, 2022

Contact Sales@multilaneinc.com for sales information.
Contact ATE-FAE@multilaneinc.com for additional technical information.

North America
48521 Warm Springs Blvd.
Suite 310
Fremont, CA 94539, USA
+1 510 573 6388

Worlwide
Houmal Technology Park
Askarieh Main Road
Houmal, Lebanon
+961 81 794 455

Asia
7th Floor-2, No. 156
Sec. 2, Dongda Road, North District,
Hsinchu City 300, Taiwan (R.O.C.)
+886 3 5744 591

UAE
Building 4WA, Office 420
Dubai Airport Freezone Authority,
Dubai, UAE
+971 4 548 7 547