400G Host Testing Solutions

Rev. 2.0

Outline

- Company Profile
- Host Testing Snapshot and Life Cycle
- ML4039EN Overview
- Engineering Characterization
  - TX Compliance
  - RX Tolerance
  - Diagnostic Validation
- Production Testing
  - Thermal Loading
  - Port Validation
- Deployment and Installation
  - CMIS Compliance
  - CMIS Interoperability
- Field and RMA Support
  - SI Troubleshooting
- Instrument Specifications

Company Profile

Our products

Interconnects

Form factors available:

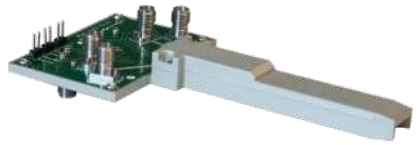
- CFP
- CFP2-DCO
- CFP2-ACO
- CFP4
- CFP8
- MicroQSFP
- QSFP-DD
- QSFP28/56
- QSFP+
- OSFP
- SFP-DD
- SFP28/56
- DSFP

Types:

- MCB
- HCB
- Loopback/ Thermal load

ML4062-TL

ML4022-MCB



ML4019-HCB

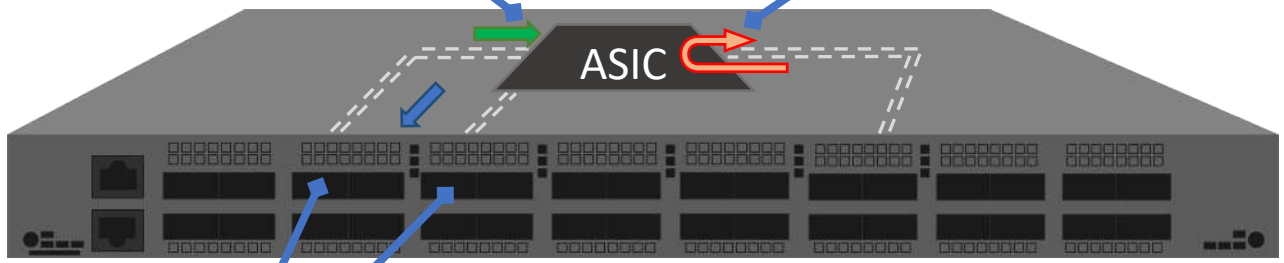
Host Testing Snapshot

RX Tolerance

Can ASIC recover noisy/jittered input signal?

Diagnostic Validation

Can ASIC execute diagnostic functions like shallow loopback, PRBS and reporting of FEC statistics?

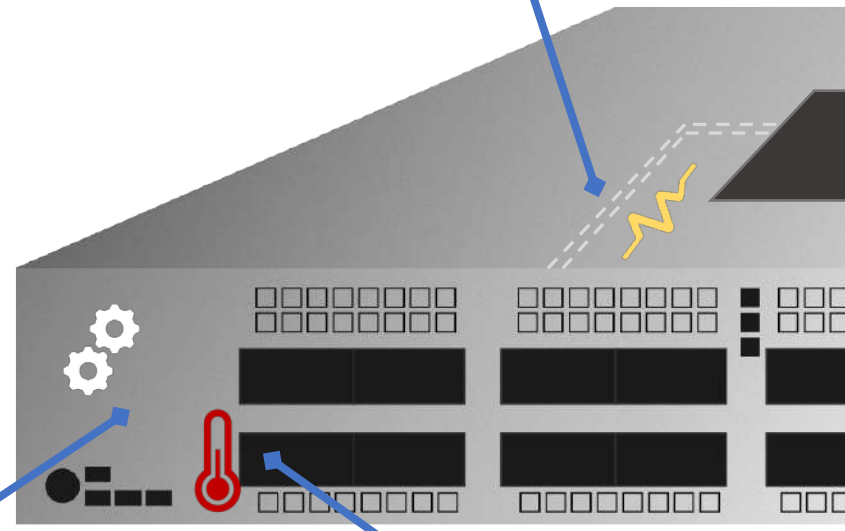


TX Compliance

Is transmit signal quality consistent from port to port?

Trace SI Troubleshooting

Is ASIC-to-port path free of impedance mismatches?



Interoperability

CMIS Compliance

Is module management robust enough for stateful host/pluggable interactions?

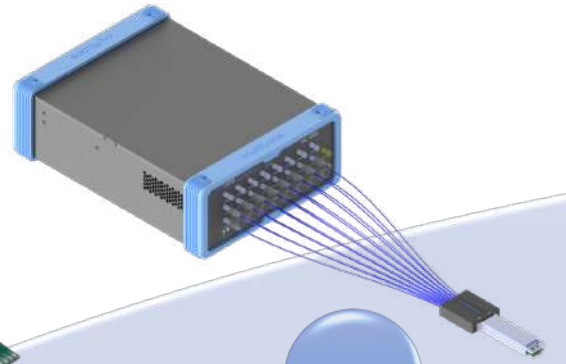
Thermal Loading

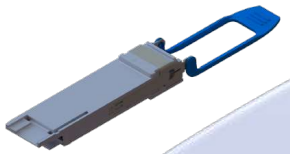
Port Validation

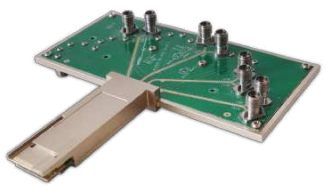
Can port function as expected and regulate pluggable temp?

Host Life Cycle

From Benchtop to Data Hall







Engineering Characterization

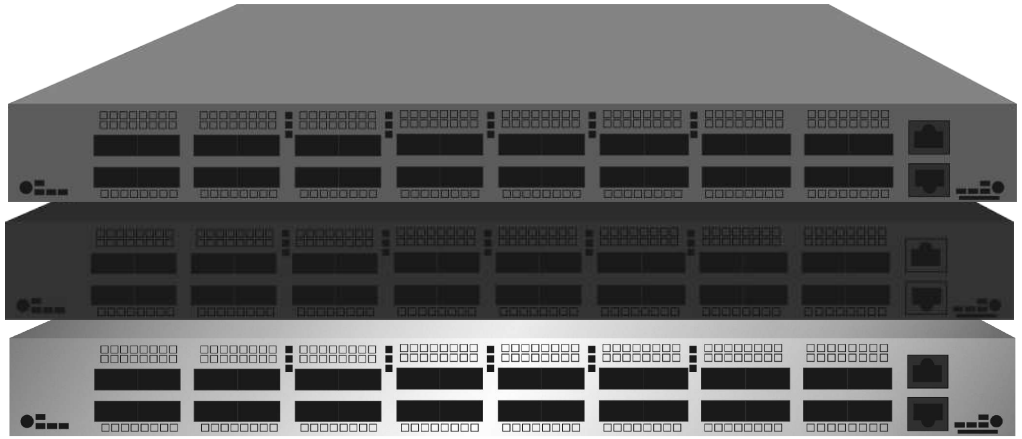
- TX Compliance
- RX Tolerance
- Diagnostic Validation

Production Testing

- Thermal Loading
- Port SI Validation

Deployment & Installation

- CMIS Compliance
- Interoperability



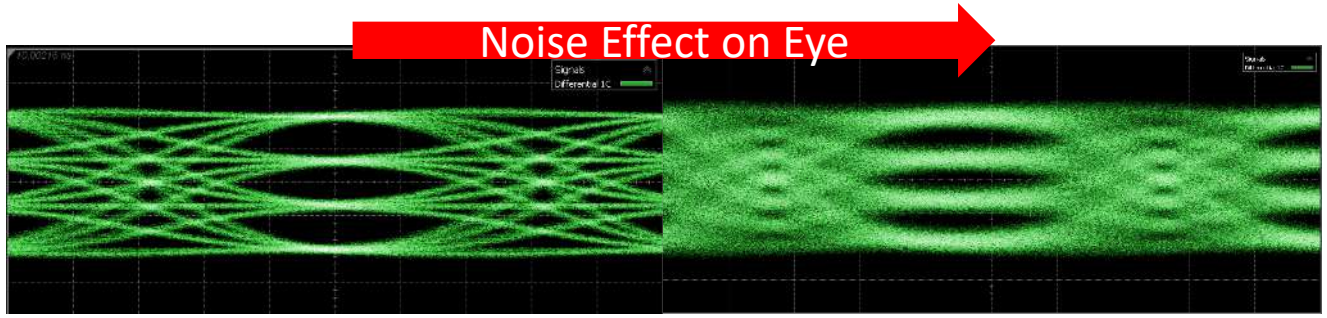
Field & RMA Support

- Port/Trace SI Troubleshooting

ML4039EN Overview

Emulate Real-Life Crosstalk Conditions

- 4x56 GBaud BERT with Crosstalk Noise Injection
- Noise implementation:
  - Continuous interference (bounded uncorrelated noise BUN, spectrum 0.5 to 20 GHz)
  - Burst crosstalk noise (140 MHz to 5 GHz repetitive, 20 GHz spectrum)
  - Single shot noise (5 ms or slower per incident)
- Real HW FEC (KP, KR) Analysis
- Programmable channel emulation (ISI impairment)
- Shallow loopback support within instrument



Engineering Characterization

Transmit Compliance

RX Tolerance

Diagnostic Validation

TX Compliance: Configuration 1

Using ML4025 and ML4039 (as CDR)

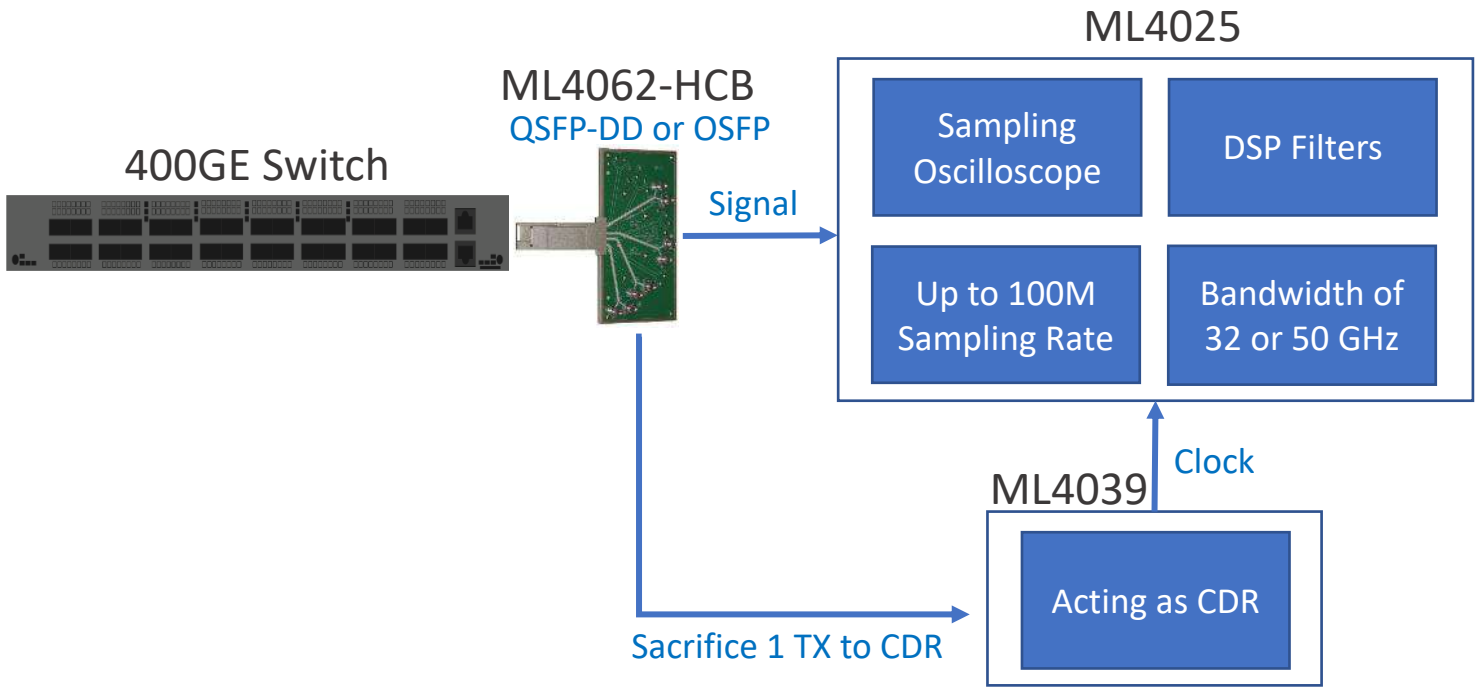
Feasible Tests

Table 120D–1—200GAUI-4 and 400GAUI-8 C2C transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)		26.5625 ± 100 ppm	GBd
Differential peak-to-peak output voltage[a] (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage[a] (max)	93.8.1.3	1.9	V
Common-mode voltage[a] (min)	93.8.1.3	0	V
AC common-mode output voltage[a] (max, RMS)	93.8.1.3	30	mV
Differential output return loss (min)	120D.3.1.1	Equation (120D–2)	dB
Common-mode output return loss (min)	93.8.1.4	Equation 93-4	dB
Output waveform[b] Level separation mismatch ratio R_{LM}(min) Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 120D.3.1.2 120D.3.1.4 120D.3.1.4 120D.3.1.4 120D.3.1.5 120D.3.1.5	 0.95 0.6 0.4 0.76 × v_f Table 120D–2 Table 120D–3	 — V V V — —
Signal-to-noise-and-distortion ratio SNDR (min)	120D.3.1.6	31.5	dB
Transmitter Output residual ISI SNR_{ISI} (min)	120D.3.1.7	34.8	dB
Output jitter J_{RMS} (max) J4u (max) Even-odd jitter (max)	 120D.3.1.8 120D.3.1.8 120D.3.1.8	 0.023 0.118 0.019	 UI UI UI

[a]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[b]The state of the transmit equalizer is controlled by management interface.

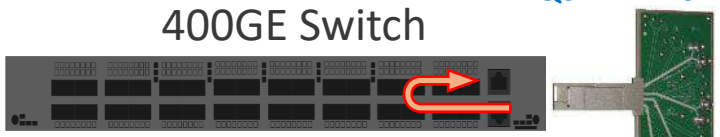
- Host ASIC enables PRBS
- Characterize TX Path with ML4025 and ML4062-HCB
- Recover clock from 1 TX Channel using CDR

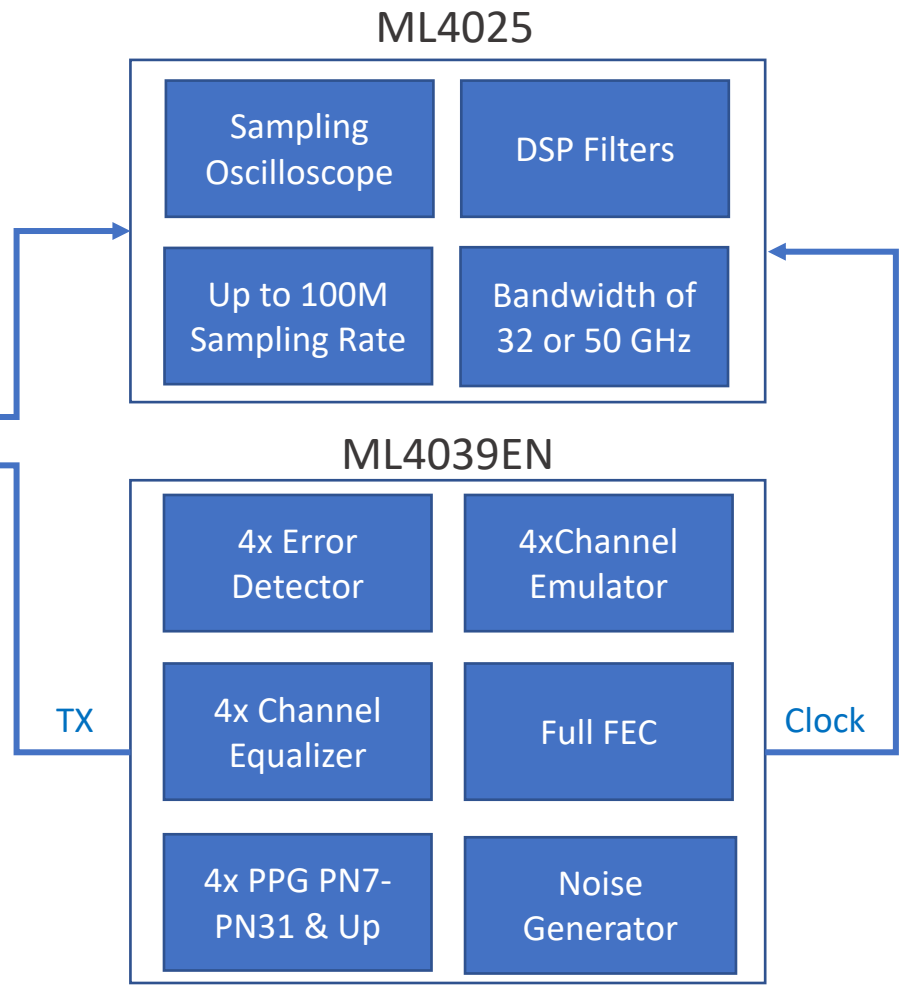


TX Compliance: Configuration 2

Using ML4025 and ML4039EN

- Access port via HCB
- Transmit signal from ML4039EN PPG
- Enable loopback within host



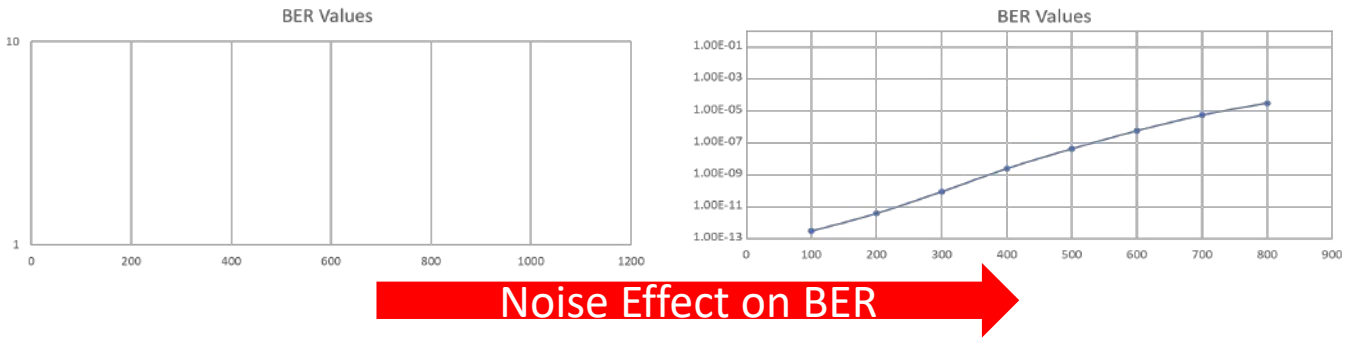


- Capture eye measurements via ML4025:
  - Eye Mask
  - Eye Amplitude
  - Eye Height
  - Eye Width
  - Jitter
  - Noise
  - Extinction Ratio
  - VEC
  - Rise/Fall Time

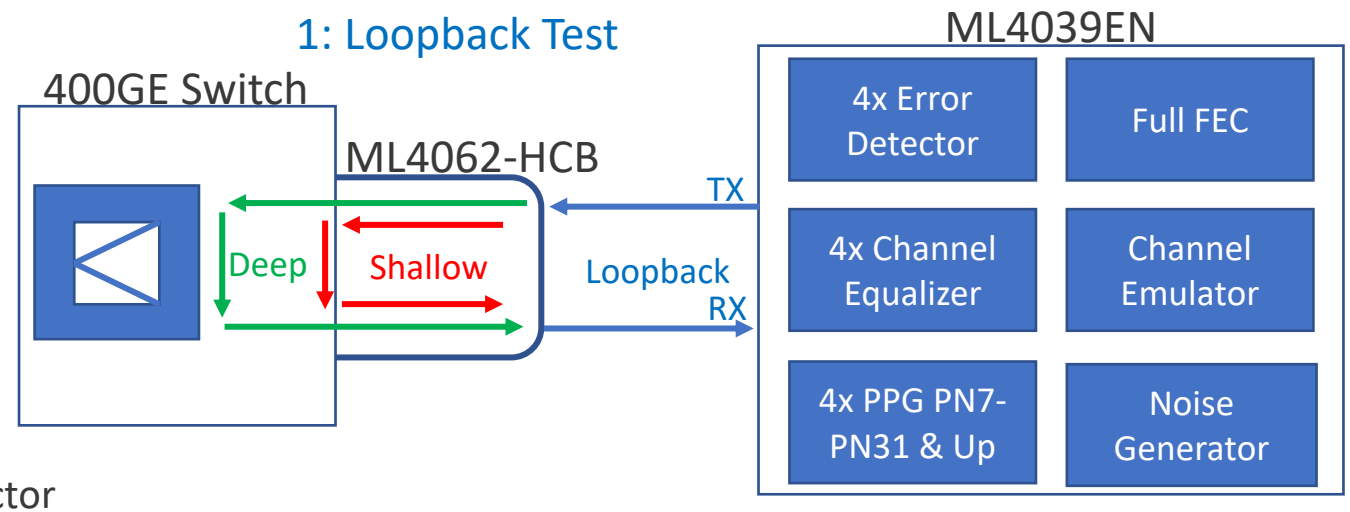
RX Tolerance

Noise Injection

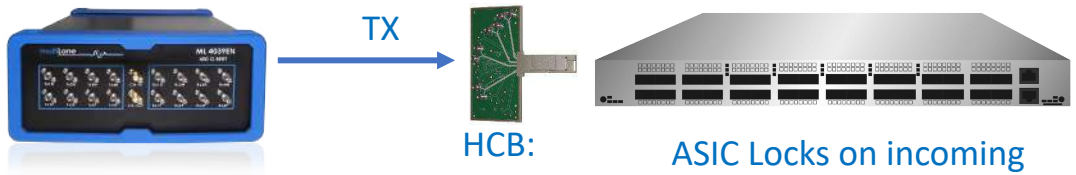
- Characterize path from Port to ASIC
- Config 1:
  - Generate noisy signal from ML4039EN PPG
  - Loop signal through switch
  - Track pre/post FEC statistics via ML4039EN Error Detector
  - Adjust multiple equalization knobs from BERT
- Config 2:
  - Generate noisy signal from ML4039EN PPG
  - Switch ASIC RX locks on incoming PRBS and reports BER



1: Loopback Test



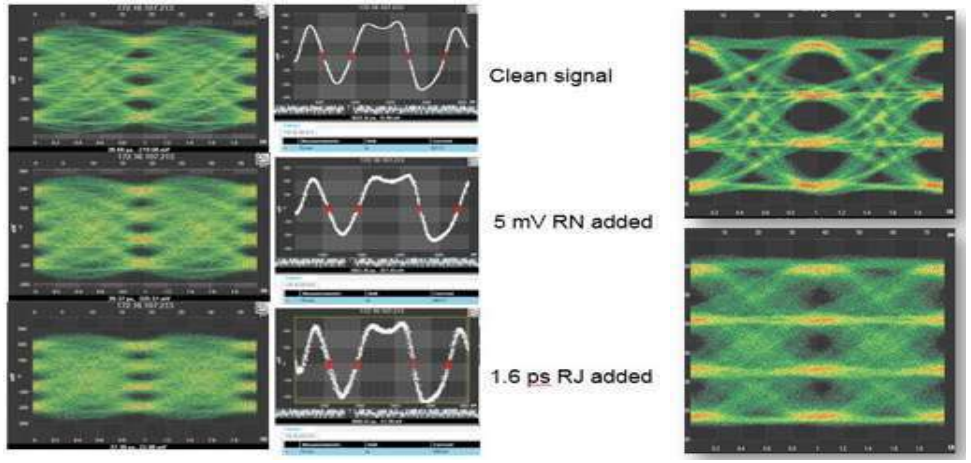
2: Single Direction Test

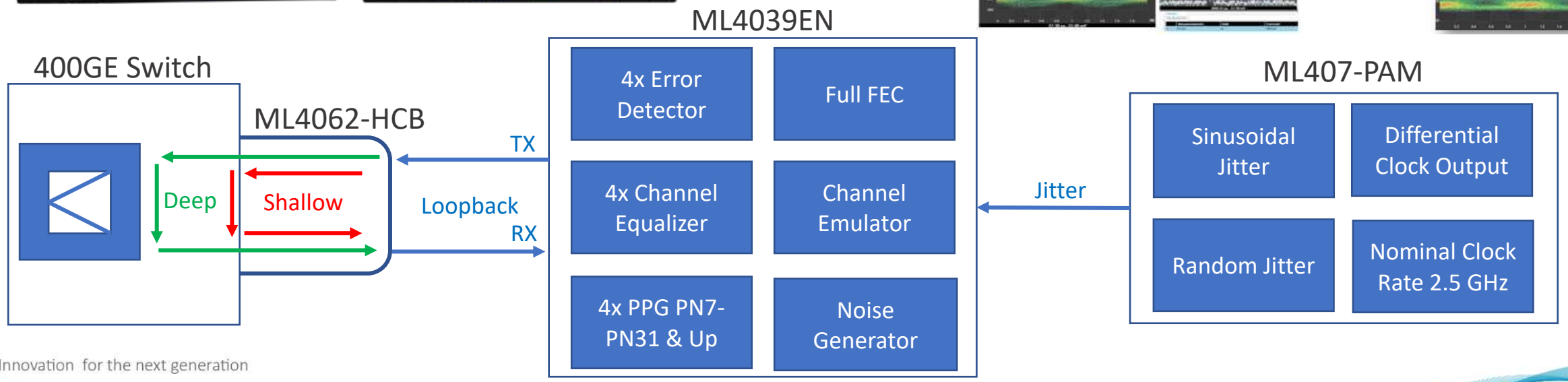


RX Tolerance

Jitter Injection

- ML407-PAM Clock Source injects SJ and RJ into ML4039EN
- Characterize host environment with simultaneous noise and jitter injection





RX Tolerance

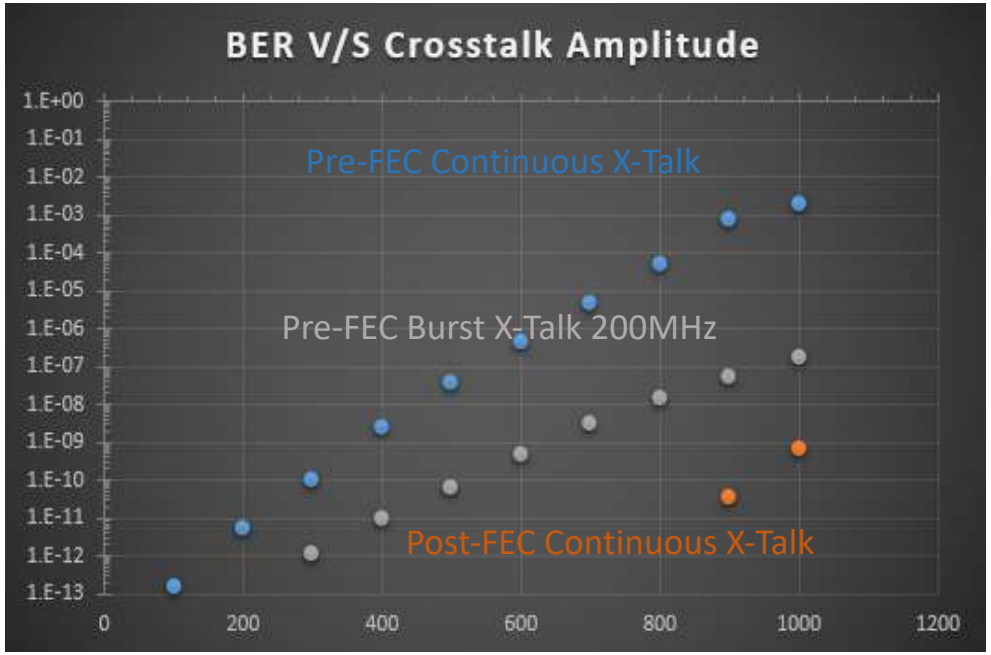
DAC Approach

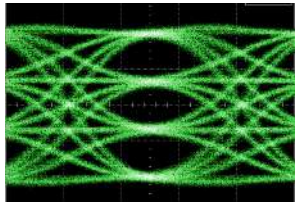
- Emulate a “Worst case channel”
- ML4039EN acts as PPG with noise injection
- ML406–MCB acts as host for 400G Direct Attach Cable (DAC)
- DAC mates with MCB and Switch port
- Bi-directional testing:
  - TX from ML4039EN PPG, RX lock via Switch ASIC
  - TX from Switch ASIC, RX lock via ML4039EN Error Detector

Diagnostic Validation

Shallow Loopback with ML4039EN

- Transmit desired traffic type within host ASIC
  - Unframed PRBS, FEC traffic,
  - Access entire port with ML4062-BO
- ML4039EN loops back switch output and injects noise
- Monitor statistics vs noise amplitude from switch CLI:
  - Pre-FEC BER (PRBS Traffic)
  - Corrected/Uncorrected Blocks (FEC Traffic)

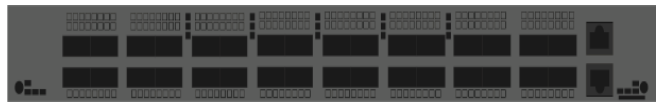




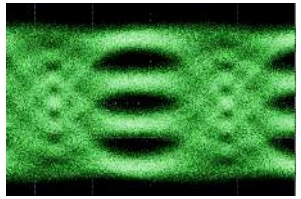
Switch Traffic

Shallow Loopback

400GE Switch



Stressed Switch Traffic



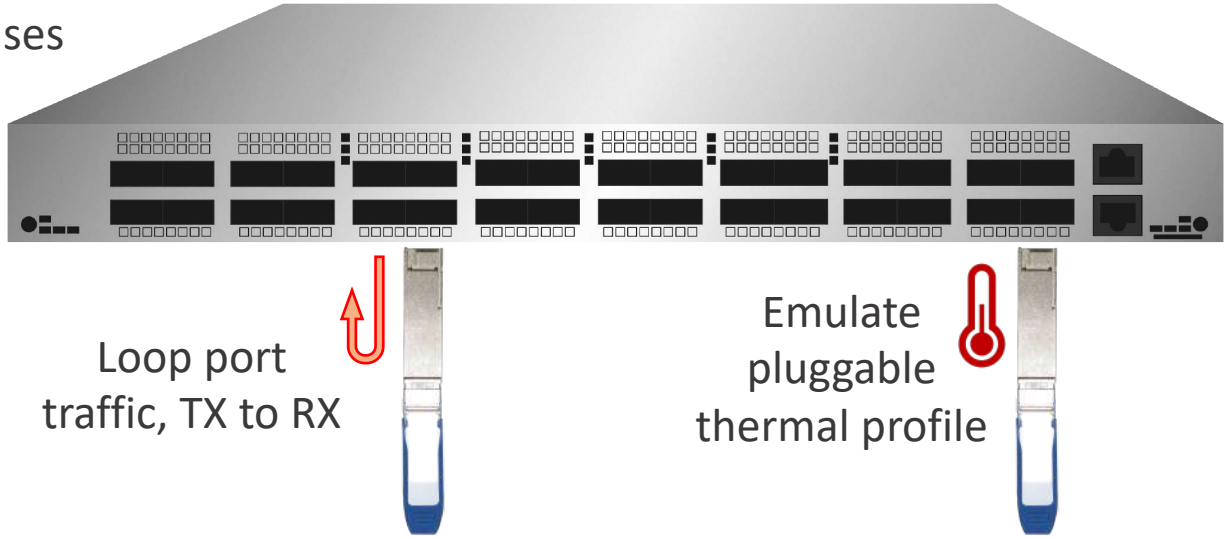
Production Testing

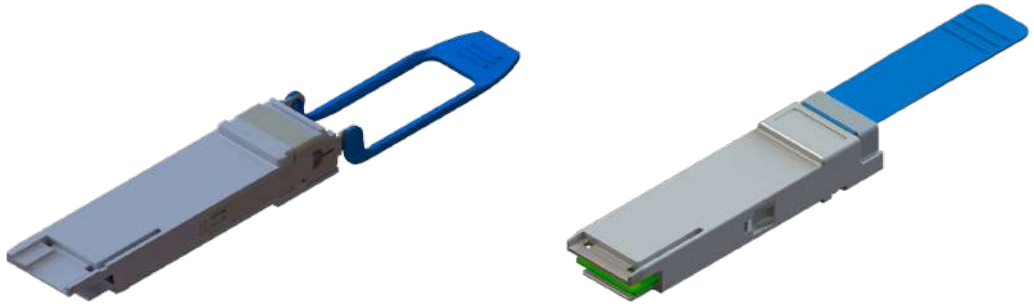
Port Validation and Thermal Loading

Pluggable Loopbacks

Industry Leading Port Testing Solutions

- MultiLane is the **global leader** for loopback solutions
- Certify port performance for production or benchtop cases
- SI traces loopback Port TX into RX
- MSA Housing Compatible
- Programmable thermal emulation:
  - OSFP (up to 24W)
  - QSFP (up to 8W)
  - QDD (up to 20W)
- Customize <u>anything</u>:
  - Insertion Loss
  - Power Dissipation
  - EE-PROM Content
  - FW for CMIS Testing
  - PN, Logo, Pull tab





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Deployment and Installation

CMIS Compliance and Interop

Smart Loopbacks

Intelligent Features via the ML4062-TL2a

- QSFP-DD MSA form factor
- MSA compatible configuration and EEPROM
- Programmable MSA memory pages
- Custom memory maps
- Low speed signal status
- Digital state decision and edge detection of control signals
- Force alarm signals to Hi/Lo or tri-state
- Three options:
  - ML4062-TL2a-C-LCD: temperature and other monitoring values (current or voltage), depending on the LCD control register
  - ML4062-TL2a-C-LED: power mode and alarms monitoring (red & green indicators with solid & blinking modes)
  - ML4062-TL2a-C-CON: board to board connection

4 Temp. Sensors | Voltage Sensor | Current Sensor

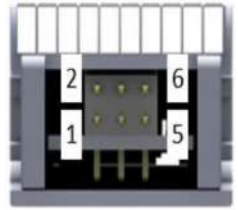
LCD Display

Led Indicator

Pin Header

Monitored LCD | R & G Indicators | Alarm System

Pin header connector

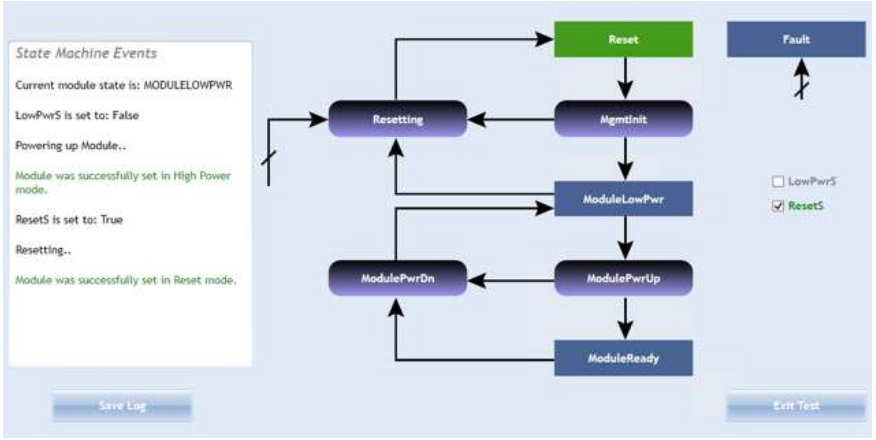


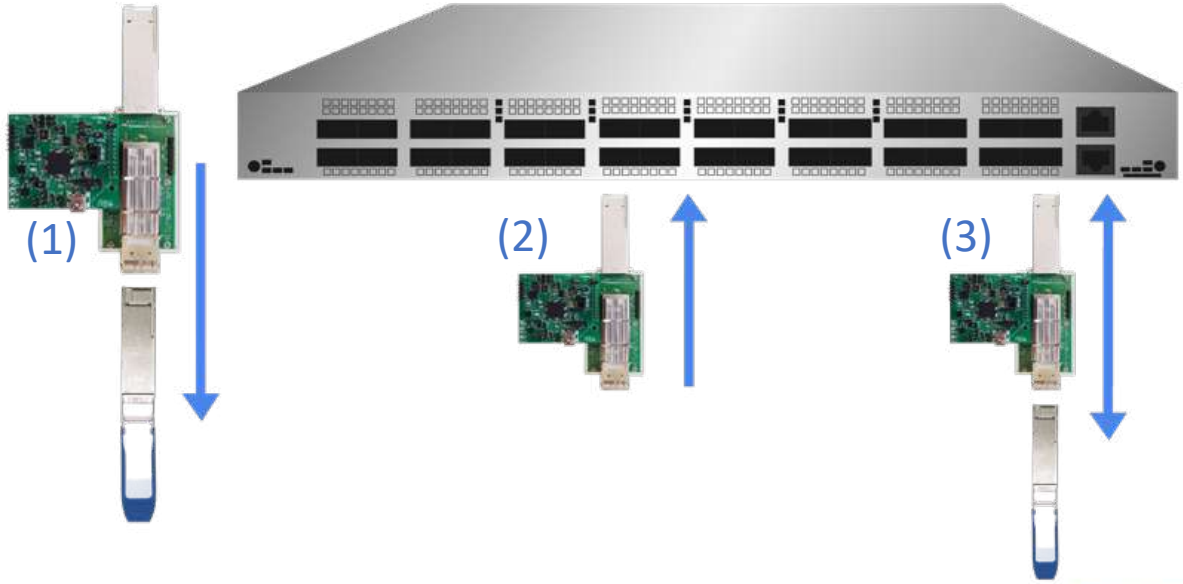
LCD power state indicator

CMIS Test

Using ML4066 Analyzer

- Validate host implementation of Common Management Interface Specification
- Certify that parameters like optic DOM and ID, errors and alarms are monitored correctly on host
- State Machine test (Pass/Fail)
- Monitor and log I2C transactions between host and pluggable
- Force host alarms
- Enable versatile CMIS testing in three modes:
  1) Master mode: Analyzer behaves as a host for a module DUT
  2) Slave mode: Analyzer behaves as a module for a Switch DUT
  3) Bypass/Sniffer mode: Analyzer reports on communication between module and switch





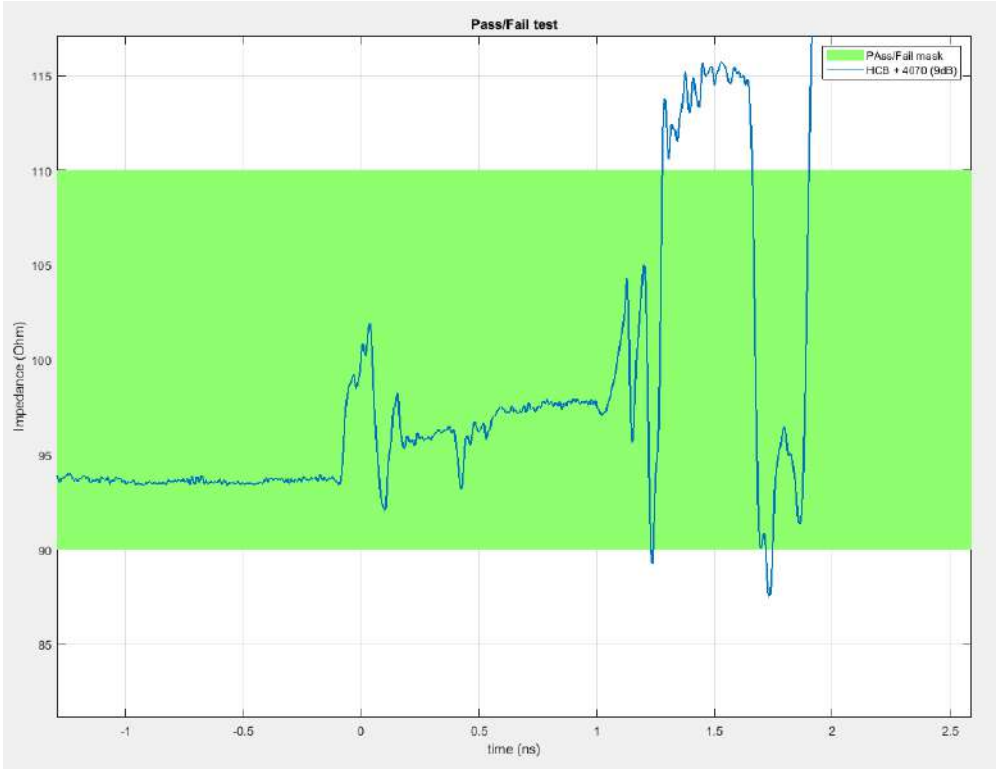
Field and RMA Support

SI Troubleshooting

Port Troubleshooting

Process Flow For Port Debug

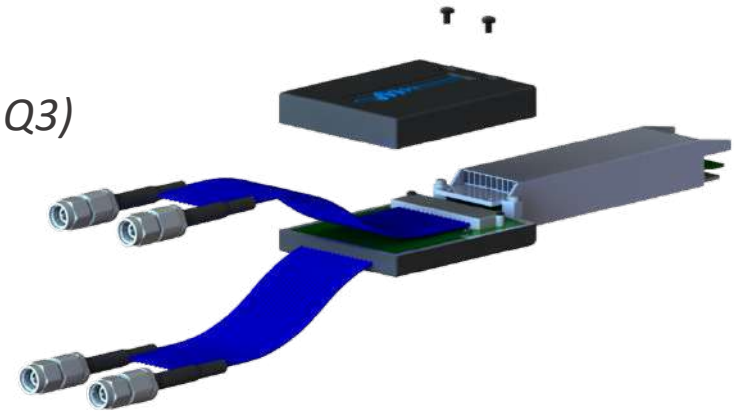
- Loopback module is first inserted for BER test
- If port BER is high, troubleshooting required
- TX path is tested using **ML4035** Scope with CDR via HCB
- Impedance measurements help identify source of issue
- The **ML4035** enables **TDR Testing** for port debug:
  - Isolate impedance mismatches and discontinuities
  - Pass/Fail verdict for each lane
  - Gated TDR → hone-in on fault area
    (for instance, a bad connector or broken pin)
  - Sub ohm accuracy
  - ~1 mm resolution

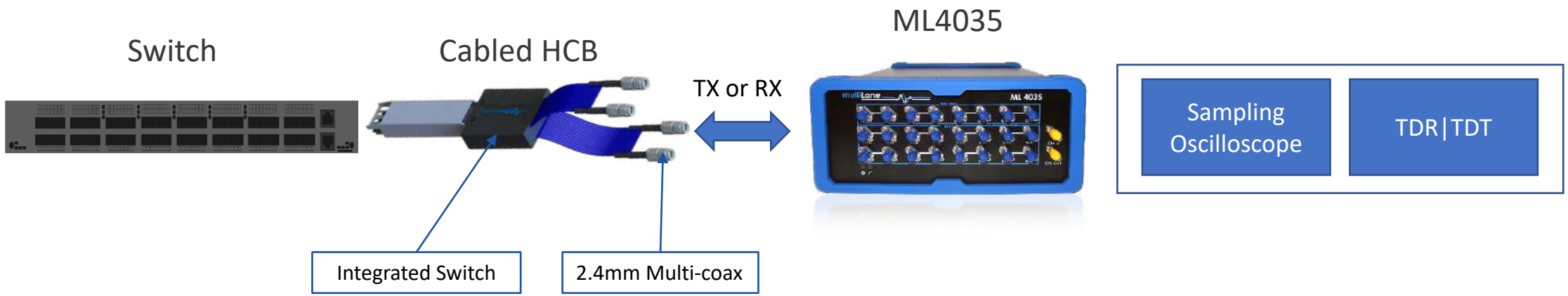


Port Troubleshooting

Introducing Cabled HCBs

- Cabled HCB: Transceiver-like connector with 2.4mm multi-coax cables *(available in Q3)*
  - RF cables and host plug integrated into one package
  - Plugs directly into switch
  - All major form factors (SFP, QSFP, QSFP-DD, OSFP & CFP2)
- Cabled HCB with integrated Switch *(available in Q4)*
  - Four integrated 4:1 switches -> Test 16 differential lanes with a 4-lane tester
  - Unlocks full port coverage (TX+RX) with a single plug





Port Characterization & Troubleshooting

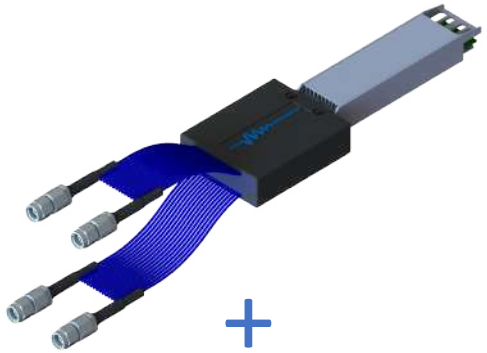
Solution Guide

Today

+

ML4035 + HCB & Cables

Q3 2020



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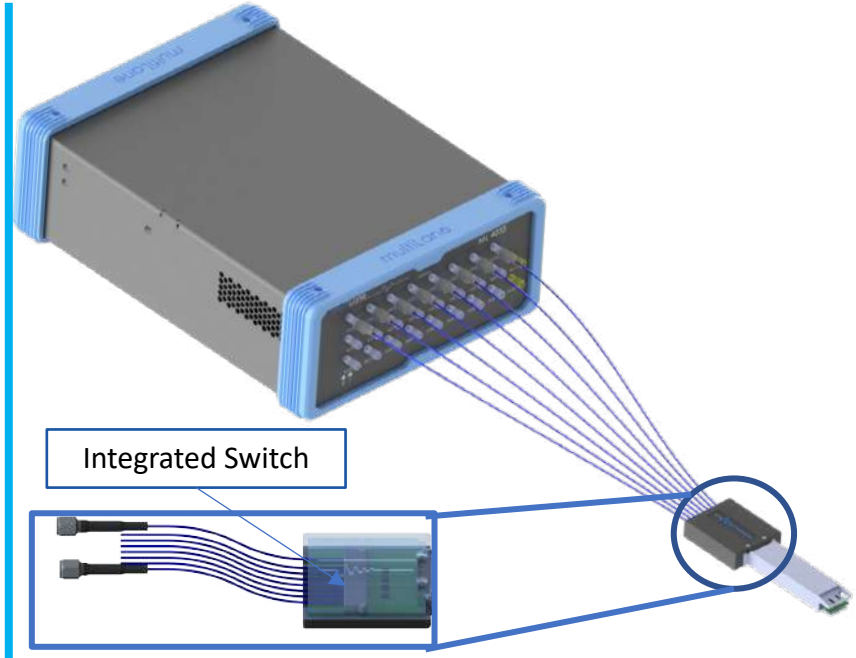
ML4035 + Cabled HCB

Q4 2020



ML4035 + Cabled HCB with Integrated Switch (single plug)

Instrument Specifications

ML4039EN Specs

- **PPG Specs**
  - NRZ & PAM4
  - Quad 23 – 29 GBd and 46 – 58 GBd
  - Full FEC (KP4 & KR4) and Gray coding
  - 3 types of noise generation:
    - Random noise (bounded uncorrelated noise BUN, spectrum 0.5 to 20 GHz)
    - Burst Noise (140 MHz to 5 GHz repetitive, 20 GHz spectrum)
    - Single shot noise (5 ms or slower per incident)
  - Channel & ISI emulation
  - 7 FIR TX taps
  - PRBS 7, 9, 13, 15, 23, 31, 58 PRBS 13Q, 15Q, 31Q SSPRQ, square & custom pattern
  - Maximum voltage swing :
    - 0 – 800 mVpp
  - Error insertion
  - Pre- and Post-emphasis

ED Specs

- Total DFE/FFE/CTLE equalization up to 13 dB
- FEC measurements (including Pre & Post FEC)
- ADC based
- SNR & PAM4 histogram monitoring
- PAM4 slicer threshold adjustable
- PRBS 7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recovery
- 4 channels of the CDR can be used to track 4 signals on the same clock with different skew, but there is one recovered clock from either of the 4 signals
- 15 FFE RX taps
- BER counters

ML4025 Specs

- 4 channel 32 or 50 GHz DSO
- Fast acquisition, FPGA-based
- Input swing max: 1200 mVpp
- Full Eye and mask measurements
- SSPRQ & up to PRBS16 pattern lock
- Jitter Decomposition (TJ, RJ, DJ)
- CTLE, S2P De-embedding, FFE, DFE, etc…
- NRZ and PAM measurement Libraries (APIs)
- Memory depth: 2^{16} Pattern Length
  - Fast acquisition
  - Full Eye and Mask Meas.
  - Fast sampling rate > 100 MHz

ML4035 BERT (PPG & ED) Specs

PPG Features

- PAM-4: 22 – 29.6 and 48 – 56 GBd
- NRZ: 22 – 29 and 48 – 56 Gbps
- DFE Pre-coding and Gray coding
- Channel Emulation & Full FEC
- PRBS 7/9/11/13/15/16/23/31/58 PRBS13Q, 31Q and SSPRQ Square wave, JP03A/B, CID JTOL pattern
- Maximum voltage swing:
  - 0 – 800 mVpp
- Error insertion
- Pre- and Post-emphasis

ED Features

- Total DFE/FFE/CTLE equalization up to 13 dB
- SNR & PAM4 histogram monitoring
- FEC measurements
- PAM4 slicer threshold adjustable
- Reference clock output rate div 8/16/32/165
- PRBS 7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recover
- BER counters

ML4035 DSO & TDR Specs

DSO Specs

- 4-Lane 35 GHz Digital Sampling Scope optimized for high speed data analysis
- High fidelity signal capture
- CDR up to 30 Gbps
- Low intrinsic Jitter
- Jitter decomposition (TJ, RJ, DJ)
- CTLE, S2P De-embedding, FFE, DFE, etc…
- SSPRQ & up to PRBS16 pattern lock
- NRZ and PAM measurement Libraries (APIs)
- Memory depth: 216 Pattern Length
  - Fast, coherent acquisition
  - Full Eye and mask measurements
  - Fast sampling rate

TDR Specs

- High resolution TDR/TDT measurements
- 4-Lane 35 GHz Time Domain Reflectometry / Transmission optimized for high speed tests and measurements
- Impedance profile measurement
- S-Parameters:
  - Return & Insertion loss
  - Crosstalk
  - Accurate multisport S-parameters

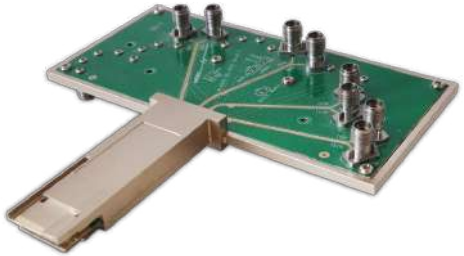
ML407-PAM Specs

- Clock source
- Sinusoidal jitter generation
- Multi-UI clock frequency
- Modulation
- Random Jitter Generation
- Used for stressed input testing of PAM4 receivers / 56G VSR PAM

Note: Anything above 4MHz is not added sine wave, but more of a flat noise

ML4062 MCB & HCB Specs

ML4062-MCB	ML4062-HCB (1&2)	ML4062-MCB-112 *(available in July)*	ML4062-HCB-112 (1&2) *(available in July)*
QSFP-DD *(Also available in OSFP)*			
8x50 Gbps	Each HCB supports 4x50G	8x112G	Each HCB supports 4x112G
2.9mm K Connectors		2.4mm V Connectors	



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THANK YOU

Innovation for the next generation

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